

# Hardware | Framegrabber | Vision Boards

# **SILICONSOFTWARE**

V-Series Camera Link



# microEnable 5 VD8-PoCL

High-speed image processing board for Camera Link

Camera Link is still a highly accepted and robust industry standard for the Machine Vision industry. Due to the availability of high-speed color cameras, based on the use of Bayer color filter arrays on greyscale sensors, and the need for advanced color inspection applications, microEnable 5 AD8-PoCL offers state-of-art technology for the Camera Link standard with up to 2,55 GB bandwidth for color image data processing and transfer. The DMA3600 technology guarantees a stable data transfer, avoiding data jam and additional CPU load.

The online color reconstruction from the Bayer CFA is based on a high-quality algorithm which processes the color data by a 5\*5 matrix, offering enhanced color quality in comparison to hardware and software solution in the market. microEnable 5 AD8-PoCL is worldwide the fastest frame grabber for color image acquisition and preprocessing for Camera Link.

For implementing customized image processing the vision FPGA is able to be programmed with the graphical tool VisualApplets. The microEnable 5 VQ8-CXP6D is pre-licensed for VisualApplets (Base) and SmartApplets (Base).

The trigger system of the microEnable 5 owns a wide functional range and high performance. As a result the user gains high flexibility and adaptability even for sophisticated requirements in complex system setups. The board is delivered with Silicon Software's runtime environment including a comprehensive SDK.

.amei	ra Interface		
Ca	amera Link	Link	
/ Po	ower over Camera Link	BCL	
С	CoaXPress		
Po	ower over CoaXPress (PoCXP)		
Ca	amera Link Standards		
	BASE Configuration		
	Dual BASE Configuration		
	MEDIUM Configuration		
~	FULL Configuration		
	0		

Υ.	10taps	FULL	Configuration

#### **Camera Connector Interface**

#### **Camera Link Connectors**

MDR26 2 SDR26

**BNC with PoCXP Support** 

DIN 1.0/2.3 with PoCXP Support

PC Interface					
4	PCI Express			PCI	
		PCIe x4 (Gen 2)			
		PCle x8 (Gen 2)			

#### **Connectivity Features**

Trigger/GPIO Connector Power Connector (PoCL)

Acquisition Features					
4	Ca	amera Pixel Clock Support			
	•	85 MHz			
1	Ca	mera Support			
	•	1* Full Configuration/Deca Mode			
1	Area Scan Cameras				
	•	16k * 64k max. image size			
1	Lin	e Scan Cameras			
	•	16k max. image width			
1	Grayscale Cameras				
	•	8bit resolution*			
	•	16bit resolution*			
1	Colo	or Cameras (*requires VisualApplets)			
	•	24bit resolution (RGB)*			
	•	48bit resolution (RGB)*			
	•	24bit resolution (Bayer CFA)			
	•	36bit resolution (Bayer CFA)*			
4	Mi	xed Mode (*requires VisualApplets)			
	•	Area Scan + Line Scan Cameras*			
	•	Grayscale + Color Cameras*			
		Arbitrary Combinations*			

# AddOn Products

- Trigger/GPIO Boards
- Trigger/GPIO Boards, opto-isolated

# Physical Board Properties

- 168 mm length x 111 mm height
- Operating temperature 0°C 50°C

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**Product Features** 

Acquisition Buffer

1 GB DDR3-RAM

**FPGA System Processor** 

**FPGA Vision Processor** 

3,6 GBytes/sec.

Sustainable Transfer Rate (max.)

DMA3600 Technology DMA3600

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Any information without obligation. Technical specifications and scope of delivery are liability-free and valid until revocation. Mistakes are excepted

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**Operation Systems** 

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# Image Acquisition Features

- High image processing and transfer performance of up to 3\*850MB/s=2,55 GB/s
- Real-time color interpolation onboard
- Support of high-speed line scan color cameras (e2v, Basler, Dalsa)
- Support of high-speed Bayer CFA area scan cameras up to CL-Deca/80bit
- Sensor Tap Sorting
- Knee Lookup Table
- Regions of Interest (ROI)
- Camera Detection Abilities
- No Need of Camera Configuration Files
- Support of Camera Link RS232 Interface clser
- Highly Customizable Trigger System
   ... and further ones

# **Special Features**

- Shaft Encoder A/B Support (Revolving Direction Detection and Compensation)
- Software Trigger Control
- Support for Non-Standard Formats
   ... and further ones

#### Software Products

- Device Drivers
- 🧹 🛛 Firmware Flasher
- microDisplay
- microDiagnostics
- microEnable SDK

Processing Libraries (V-Series)			
incl.		Acquisition Applets	
incl.		SmartApplets Base	
	opt.	SmartApplets Extended	
	opt.	SmartApplets 3D	
incl.		VisualApplets Base	
	opt.	VisualApplets Libraries	

# Processing Licenses (Base version, V-Series) SmartApplets enabled VisualApplets enabled



Supported Features Sorted by Acquisition Applets for			∞		8 (Opt 1)
microEnable 5 VD8-PoCL (Status 07/2014)			ıll Area Bayer	lll Line Gray 8	Ill Line Bayer
		<u>ت</u>	Ľ.	<u>ت</u>	Ľ.
Camera Support	Number of cameras	1	1	1	1
	Max. camera clock [in MHz]	85	85	85	85
	Camera Link Full Configuration (8 Tap, 8bit)	•	•		•
	Camera Link Deca/80bit (10 Tap, 8bit)	•	•	•	•
Camera Type	Area Scan / Line Scan	А	А	L	L
	GrayScale / RGB / Bayer	G	G	В	В
Color Interpolation	Bayer Line (Pattern 1: two lines, first blue/red, second green/green				
	Bayer (High Quality Extended, 5*5)				
Color Processing	White Balancing				
Image Pre-processing	Knee-LUT Table (Full Resolution)	•	•	•	•
	Image Enhancements				
	Noise Filter / Median				
Image Correction	Dead Pixel Interpolation				
	Area Shading Correction (2D) - Offset and Gain				
	Line Shading Correction (1D) - Offset and Gain			•	
Signal Processing	Line Trigger				
	Area Trigger				
	I/O Boards Opto/TTL available				
Performance	Max. image width [in k pixels]	16	16	16	16
	Max. image height [in k lines]	64	64	64	64
	DMA transfer performance [in MByte/s] dependent of the PC mainboard	1600	3400	1600	3200
Image Formats	Gray8 (8bit output)				
	RGB24 (BGR, 3x8bit output)				

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