CLS-212 CAMERA LINK SIMULATOR

User's Manual

Document # 200483, Rev 1.0, 06/30/2010

418 Boston Turnpike #104 • Shrewsbury, MA 01545
Phone 508.842.0165 • Fax 508.842.8930
Email info@vividengineering.com
Web www.vividengineering.com

Table of Contents

1. Introduction

1.1. Overview

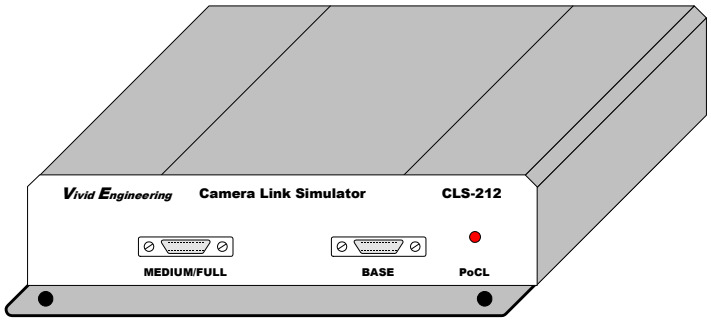
The CLS-212 Camera Link [1] simulator is a high-performance video test pattern generator supporting all Camera Link configurations (base, medium, full) plus 80-bit modes. Fully programmable video timing enables the CLS-212 to mimic the timing characteristics of Camera Link cameras with video clock rates up-to 85 MHz. The CLS-212 incorporates the Miniature Camera Link (miniCL) connector widely used in Power over Camera Link (PoCL) applications

The CLS-212 is controlled using a PC with a standard RS-232 serial port. Alternatively, the CLS-212 can be connected to a PC USB port using an optional adapter. CLS-212 control is performed via a simple, straightforward, Command Line Interface (CLI). No special software is required. Configuration files are easily created with user parameters and downloaded to the CLS-212. CLS-212 default (power-up) configuration is user programmable. This provides convenient recall of saved parameters and enables CLS-212 operation without a host computer.

The CLS-212 Camera Link Simulator is extremely useful for the development, test, and integration of Camera Link products and systems. The CLS-212 is particularly useful for testing PoCL cables and PoCL frame grabber SafePower functionality. The CLS-212 is housed in a sturdy aluminum enclosure.

---

[1] The Camera Link interface standard enables the interoperability of cameras and frame grabbers, regardless of vendor. The Automated Imaging Association (AIA) sponsors the Camera Link program including the oversight Camera Link Committee, the self-certification program, and the product registry. The Camera Link specification may be downloaded from the AIA website, found at www.machinevisiononline.org


Vivid Engineering
Camera Link Simulator
CLS-212
MEDIUM/FULL
BASE
PoCL

1.2. Features

- A high-performance video test pattern generator
- Supports all Camera Link configurations (base, medium, full)
- 80-bit mode support; ten 8-bit taps, and eight 10-bit taps
- Supports Power over Camera Link (PoCL)
- Fully programmable video timing; mimics camera characteristics
- Advanced chipset supports video clock rates up-to 85 MHz
- Area and line scan formats, image sizes to 64Kx64K
- Box, line, horizontal/vertical/diagonal wedge test patterns
- Programmable video pattern initial values and step sizes
- "Roll" feature adds pattern motion
- Triggered (exsync) mode & Integration timer
- Tests/exercises frame grabber and cable PoCL SafePower functionality
- Incoporates the Miniature Camera Link (miniCL) connectors widely used in PoCL applications.
- Connects to host PC serial port (RS-232), or USB port w/ optional adapter
- Controlled via a simple Command Line Interface (CLI), command set compatible with the non-PoCL CLS-211 simulator
- Downloadable configuration files are easily created and modified w/ user settings
- Non-volatile save/recall of user settings
- Can operate stand-alone
- Sturdy, compact aluminum enclosure w/ mounting flange

- External multi-nation power supply and RS-232 cable included
- 3-year warrantee

1.3. Functional Description

The CLS-212 Camera Link Simulator is a programmable video test pattern generator supporting all Camera Link configurations (base, medium, full), plus 80-bit modes. A block diagram of the CLS-212 is provided in Figure 1-1. Descriptions of the functional blocks are provided in the following sections.

The CLS-212 combines video test pattern generation circuits implemented in Field Programmable Gate Array (FPGA) technology with an on-board microcontroller. The FPGA-based video test pattern circuitry provides the desired video timing, active window, and test pattern characteristics. The microcontroller links the pattern generation circuitry to the host computer and incorporates a simple, straightforward Command Line Interface (CLI). This enables the CLS-212 to be controlled using any computer incorporating a standard RS-232 serial port, or USB using optional adapter. Users may interactively assign settings via the CLI, or may download configuration files created in advance. The CLS-212 incorporates non-volatile memory for storing user configuration settings. Saved settings are automatically loaded upon power-up, enabling operation of the CLS-212 using pre-loaded parameters without a host computer.

The CLS-212 Camera Link Simulator incorporates a clock synthesizer which enables the user to select virtually any test pattern clock frequency in the extended Camera Link 20-85 MHz range. The camera control inputs of the Camera Link interface are sent to timing generator for use as exsync inputs, enabling the frame grabber to trigger pattern generation and an integration timer adds camera exposure characteristics. The serial link in the Camera Link interface is looped back to the frame grabber, enabling loopback test of the serial interface.

The CLS-212 includes features for testing and exercising Power over Camera Link (PoCL) interfaces. This makes the CLS-212 particularly useful for testing PoCL cables and PoCL frame grabber SafePower functionality. The CLS-212 video connectors are the Miniature Camera Link (miniCL) type widely used in PoCL applications.

The CLS-212 camera interface incorporates the connector, signals, pinout, and chipset in compliance with the Camera Link specification. The CLS-212 incorporates the “base”, “medium” and “full” configuration signal sets, consisting of video data, camera control, and serial communications. The CLS-212 also supports two 80-bit modes; ten 8-bit taps and eight 10-bit taps.

The CLS-212 is powered by an external multi-nation wall plug-in power supply which is included. Also included is an RS-232 serial cable.

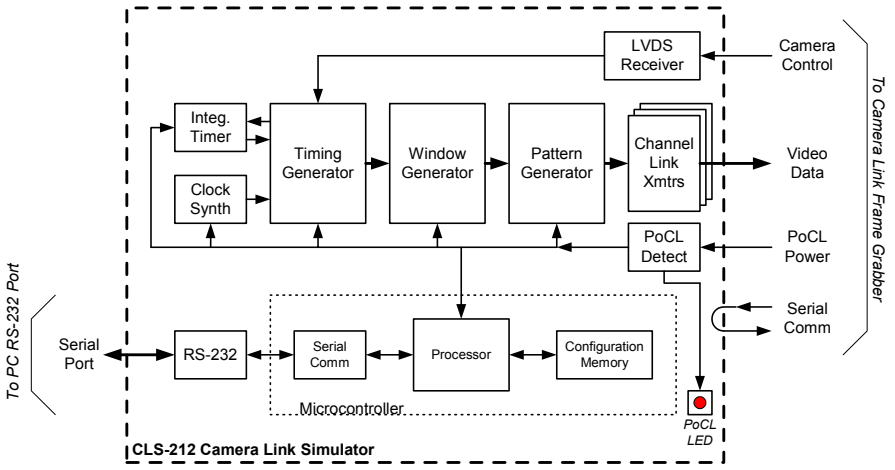


Figure 1-1: CLS-212 Block Diagram

1.3.1. Clock Synthesizer

The CLS-212 Camera Link Simulator incorporates a clock synthesizer circuit to generate the reference clock for the video test patterns. The clock synthesizer is capable of generating virtually any reference clock frequency in the extended Camera Link 20-85 MHz range. The reference clock is used by the timing, window, and pattern generation circuitry and is also sent to the frame grabber via the Camera Link interface. As with all CLS-212 user parameters, clock frequency settings are stored to non-volatile memory in response to a parameter save command. Stored clock settings are automatically retrieved from memory upon power-up, or in response to a parameter recall command. The CLS-212 clock synthesizer chip is an 307M-02LF made by Integrated Device Technology (IDT).

The CLS-212 Command Line Interface (CLI) incorporates two commands for selecting the reference clock frequency. With the *frequency* command, the user simply specifies an integer frequency between 20 and 85 MHz (i.e. 20,21,22…85).

For fractional frequencies (i.e. 27.375 MHz), the *synth_code* command allows direct input of the programming code into the clock synthesizer chip. An online synthesizer code generation tool is available on the Integrated Device Technology (IDT) website at http://www.idt.com/?app=calculators&device=307_02 Simply follow the link and enter the following parameters into the window:

- In the Input Frequency box, enter "14.31818"
- Enter desired output frequency
- Enter desired accuracy
- In the Clock 2 Output box, select "OFF"
- In the Output Driver box, select "CMOS"
- In the Crystal Load Capacitance box, select "00"
- Click on the "Calculate" button

Example: Running the tool for a desired frequency of 27.375 MHz will return several codes based on best accuracy, lowest jitter, etc. The best accuracy code is 0x248939. To load this code into CLS-212, type "SYNTH_CODE 0x248939" at the command line prompt.

1.3.2. Timing Generator

The CLS-212 Camera Link Simulator timing generator establishes the basic video timing characteristics by generating the Line Valid (LVAL) and Frame Valid (FVAL) timing signals. The circuit operates at the reference clock frequency programmed into the clock synthesizer.

LVAL is used to envelope *lines* of video data and is defined in the Camera Link specification as *high* for valid line data. Two CLS-212 timing parameters, LVAL_LO and LVAL_HI, determine the duration of LVAL low and high states in pixel clock cycles, respectively. The frequency of the pixel clock is determined by the clock synthesizer. The CLS-212 supports "LVAL low" and "LVAL high" times from 1-65535 pixel clocks. LVAL timing characteristics are shown in Figure 1-2.

Note: The LVAL timing signal is continuously output whenever the CLS-212 is operated in framescan mode. For linescan mode, LVAL is continuous when in operating in "continuous" mode. For linescan mode with exsync triggering, a single LVAL pulse is issued in response to each triggering event.

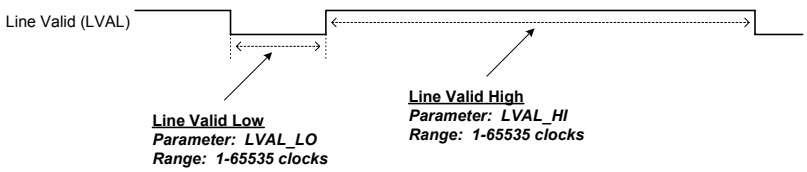


Figure 1-2: Line Valid (LVAL) Timing Characteristics

FVAL is used to envelope *frames* of video data from framescan cameras and is defined in the Camera Link specification as *high* for valid frame data. Two CLS-212 timing parameters, FVAL_LO and FVAL_HI, determine the duration of FVAL low and high states in video lines, respectively. Video lines refer to the Line Valid (LVAL) signal which was discussed in the prior paragraph. The CLS-212 supports FVAL low and FVAL high times from 1-65535 lines. FVAL timing characteristics are shown in Figure 1-3.

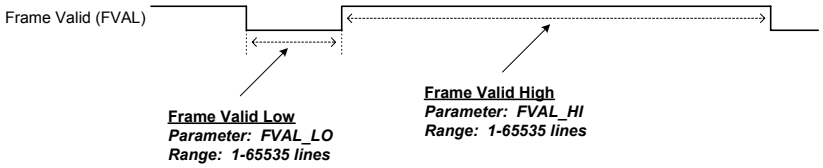


Figure 1-3: Frame Valid (FVAL) Timing Characteristics

The relative positioning of the FVAL and LVAL timing signals is programmable and is specified using the Frame Valid Setup (FVAL_SETUP) and Frame Valid Hold (FVAL_HOLD) parameters.

When FVAL_SETUP and FVAL_HOLD are both set to 0, the default condition occurs whereby transitions on the FVAL signal occur coincident with the falling edge of the LVAL signal (the start of the horizontal blank interval). This relationship is illustrated in Figure 1-4.

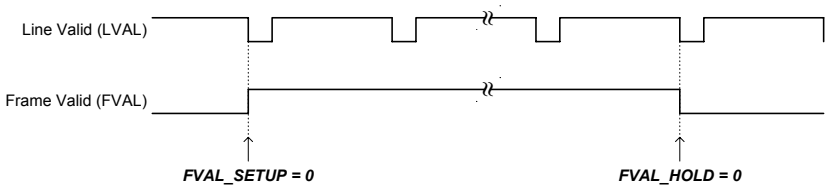


Figure 1-4: Default LVAL/FVAL Timing Relationship

The FVAL_SETUP and FVAL_HOLD parameters allow CLS-212 timing characteristics to be fine tuned in order to mimic camera characteristics, verify frame grabber functionality, etc. Figure 1-5 illustrates how a value

inserted in the FVAL_SETUP results in the rising edge of FVAL occurring *in advance of* the falling edge of LVAL. The figure also illustrates how FVAL_HOLD values result in the falling edge of FVAL occurring *after* the falling edge of LVAL.

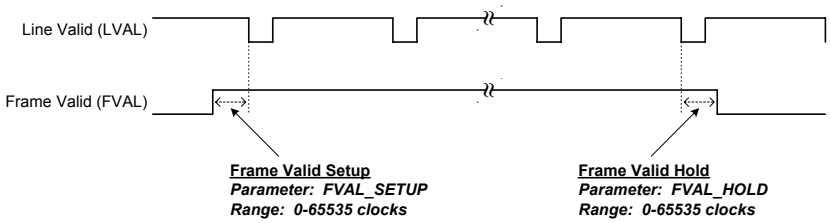


Figure 1-5: FVAL Setup/Hold Timing Parameters

1.3.3. Window Generator

The CLS-212 Camera Link Simulator incorporates a programmable window generator that determines the size and position of the video test pattern. The window generator accepts four parameters to determine the position and size of the video test pattern relative to the FVAL and LVAL timing signals described in Section 1.3.2

The starting position of the video test pattern is determined by the X Offset (XOFF) and Y Offset (YOFF) parameters. XOFF determines the staring position within a line ("x" position), and the YOFF parameter determines the starting row ("y" position).

Test pattern image size is defined using the XACT and XOFF parameters. X Active (XACT) determines the horizontal test pattern size in pixels, and Y Active (YACT) determines the vertical pattern size in lines.

Figure 1-6 shows the test pattern line positioning relative to LVAL. Figure 1-7 illustrates the window generation characteristics based on XOFF, YOFF, XACT, and XACT.

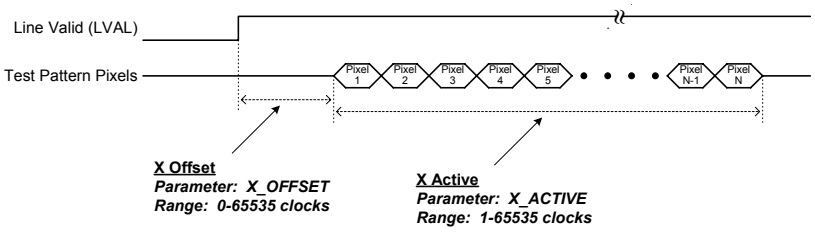


Figure 1-6: Horizontal (X) Offset/Active Parameters

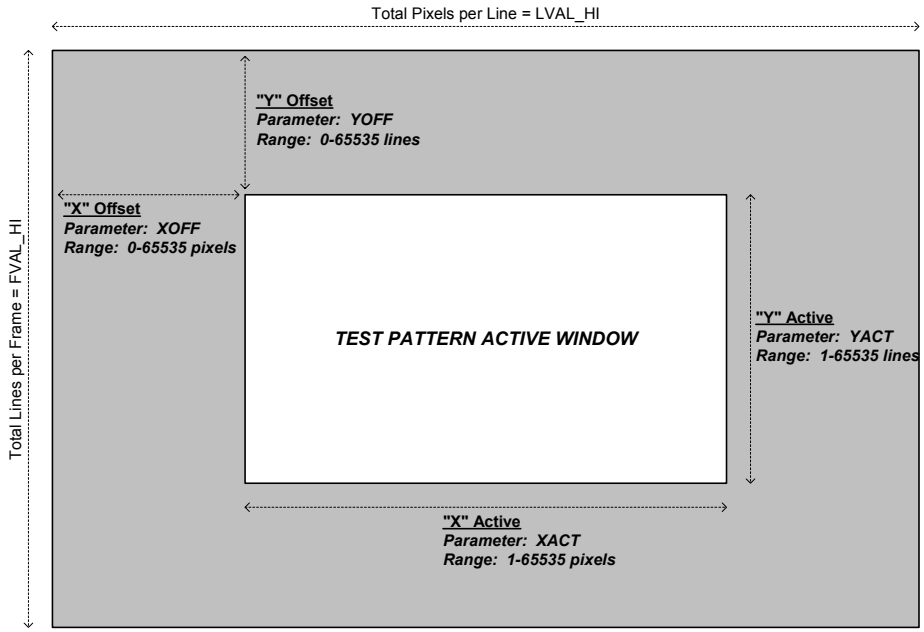


Figure 1-7: Window Generator Characteristics

1.3.4. Pattern Generator

The CLS-212 Camera Link Simulator incorporates a programmable pattern generator to create a variety of test patterns. The CLS-212 is capable of generating rectangular fixed-value, horizontal wedge, vertical wedge, and diagonal wedge patterns as shown in Figures 1-8 through 1-11. The rectangular fixed-value pattern may be any width or height (i.e. vertical line, horizontal line, dot, square, etc), in any position, and with selectable foreground and background pixel values.

The CLS-212 enables the user to individually select the test pattern for up-to ten pixel outputs (A/B/C/D/E/F/G/H/I/J/I/J) in the multi-tap and color modes. To support this feature, ten Pattern Select (A_PATSEL, B_PATSEL, C_PATSEL, D_PATSEL, E_PATSEL, F_PATSEL, G_PATSEL, H_PATSEL, I_PATSEL, J_PATSEL) parameters are provided. The PATSEL parameters are defined in Table 1-1.

Table 1-1: PATSEL Parameter Definition

Pattern Select Value (A_PATSEL, B_PATSEL, C_PATSEL, D_PATSEL (E_PATSEL, F_PATSEL, G_PATSEL, H_PATSEL, I_PATSEL, J_PATSEL)	Video Test Pattern
0	Fixed Value (rectangular)
1	Horizontal Wedge
2	Vertical Wedge
3	Diagonal Wedge

For the fixed value pattern, ten Pixel Fixed Value (A_FIXED, B_FIXED, C_FIXED, D_FIXED, E_FIXED, F_FIXED, G_FIXED, H_FIXED, I_FIXED, J_FIXED) parameters are provided to individually select static pixel values for the up-to ten pixels that are being simultaneously output.

The CLS-212 enables the user to select background pixel values. These are the default output pixel values at all times outside the active video region defined by the window generator. The CLS-212 enables the user to individually select the background value for each of the up-to ten pixel outputs (A/B/C/D/E/F/G/H/I/J/I/J). To support this feature, ten Pixel Background Value (A_BACK, B_BACK, C_BACK, D_BACK, E_BACK, F_BACK, G_BACK, H_BACK, I_BACK, J_BACK) parameters are provided.

The CLS-212 provides a selectable pixel step size when generating wedge (horizontal, vertical, diagonal) patterns. The step size determines the amount by which pixel values are incremented from pixel-to-pixel in the test patterns. The default setting of "1" causes the pixel values to increment by 1. Step sizes of 2, 4, 8, 16, 32, 64 and 128 are also supported. The pixel step size feature is particularly valuable when working with high-resolution (i.e. 12 or 16-bit) video. The CLS-212 enables the user to individually select the step size for each of the up-to ten pixel outputs (A/B/C/D/E/F/G/H/I/J). To support this feature, ten Pixel Step Size (A_STEP, B_ STEP, C_ STEP, D_ STEP, E_ STEP, F_ STEP, G_ STEP, H_ STEP, I_ STEP, J_ STEP) parameters are provided. Note that the step size applies to both the horizontal (i.e. pixel to pixel) and the vertical (line to line) directions.

When generating wedge (horizontal, vertical, diagonal) patterns, the CLS-212 enables the user to select the initial value of each pixel. This is the value associated with the first pixel in the video frame. The value then increments, according to the wedge pattern selected. The default initial values are "0". The pixel initial value feature is particularly valuable in generating wedge patterns while simulating multi-tap cameras. The CLS-212 enables the user to individually select the initial value for each of the up-to ten pixel outputs (A/B/C/D/E/F/G/H/I/J). To support this feature, ten Initial Value (A_INIT, B_ INIT, C_ INIT, D_ INIT, E_ INIT, F_ INIT, G_ INIT, H_ INIT, I_ INIT, J_ INIT) parameters are provided.

The CLS-212 "roll" feature used in conjunction with the wedge patterns (horizontal, vertical, diagonal) to introduce test pattern motion. When roll is enabled, the starting pixel value in the video test pattern increments every frame. This changes all pixel values within the pattern every frame and adds a "rolling" motion to the displayed pattern. This feature is particularly useful during testing and for debugging image acquisition problems.

The CLS-212 supports all modes defined in the Camera Link specification for the “base”, “medium”, and “full” configurations. These modes range from simple 8-bit single-tap, to 12-bits by 4-taps, to 8-bits by 8-taps. The desired mode is selected using the Camera Link Mode (CL_MODE) parameter. The CL_MODE parameter is defined in Table 1-2.

The CLS-212 supports the two 80-bit formats being added to the Camera Link Specification. Sometimes called “DECA” mode, an 8-bit by 10-tap mode is now supported. The proposed 10-bit by 8-tap mode is also supported.

For simplicity, the CLS-212 refers to A-B-C-D-E-F-G-H-I-J “pixels”, not “ports”. The CLS-212 outputs up-to ten pixels simultaneously, depending on Camera Link mode. The pixel values are automatically mapped to the corresponding port assignments as defined in the Camera Link specification.

Table 1-1: CL_MODE Parameter Definition

CL_MODE Parameter Setting (decimal)	Camera Link Mode
0	8-bit x 1~3 (base configuration)
1	10-bit x 1~2 (base configuration)
2	12-bit x 1~2 (base configuration)
3	14-bit x 1 (base configuration)
4	16-bit x 1 (base configuration)
5	24-bit RGB (base configuration)
8	8-bit x 4 (medium configuration)
9	10-bit x 3~4 (medium configuration)
10	12-bit x 3~4 (medium configuration)
11	30-bit RGB (medium configuration)
12	36-bit RGB (medium configuration)
13	8-bit x 10 (full-configuration, 80-bit, “DECA”)
14	10-bit x 8 (full-configuration, 80-bit)
15	8-bit x 8 (full configuration)

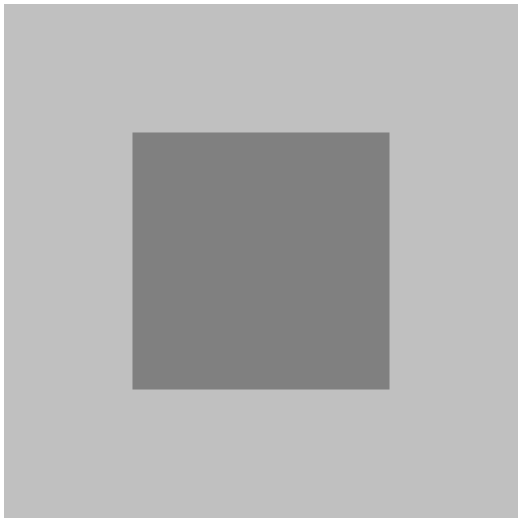


Figure 1-8: Fixed (Single Rectangle) Test Pattern

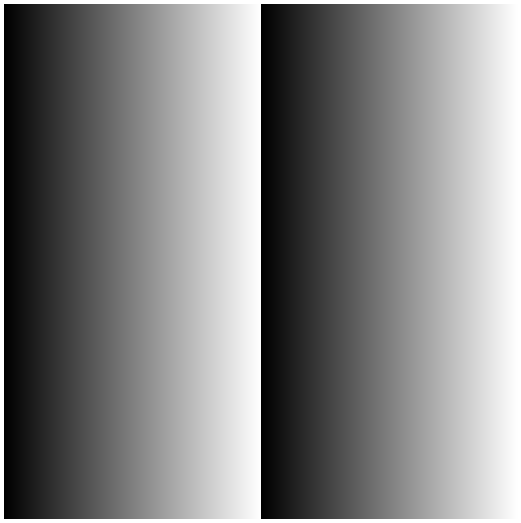


Figure 1-9: Horizontal Wedge Test Pattern

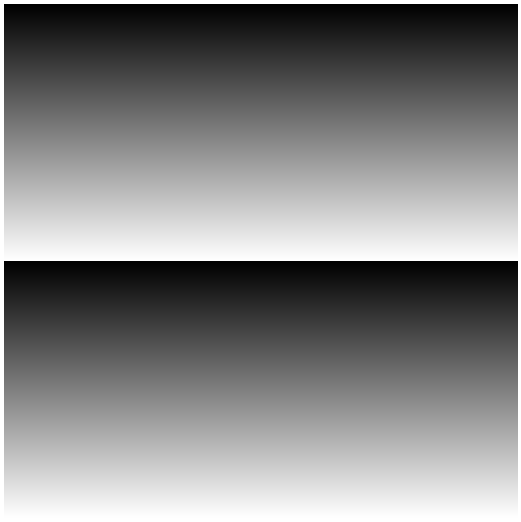


Figure 1-10: Vertical Wedge Test Pattern

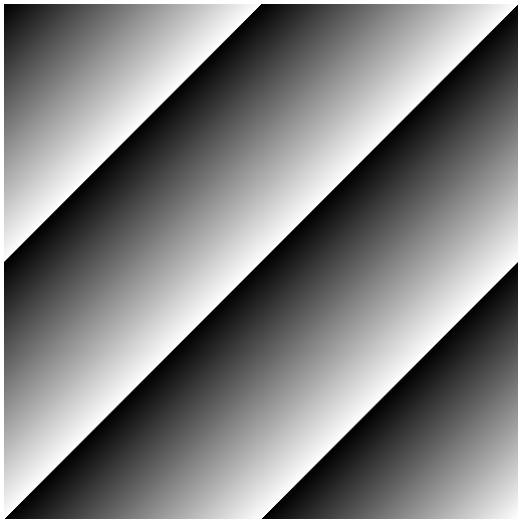


Figure 1-11: Diagonal Wedge Test Pattern

1.3.5. Data Valid (DVAL) Signal

The CLS-212 includes features to mimic low-speed cameras which utilize the Data Valid (DVAL) signal in the Camera Link interface. Camera Link requires a minimum pixel clock rate of 20 MHz. To support cameras and sensors with pixel rates below 20 MHz, the Camera Link interface provides the Data Valid signal which qualifies the data received from the camera. This capability enables a camera to provide a pixel clock of at least 20 MHz, but qualify only a portion of the data sent, effectively providing a sub 20 MHz pixel clock.

The data valid features are controlled using the DVAL and DVAL_MODE control registers. When DVAL_MODE is set to 0, activity on the DVAL signal is disabled and DVAL is held at the static state specified by the DVAL control register. When DVAL_MODE is set to 1-3, the DVAL signal is active (high) every 2nd, 4th, or 8th clock cycle. Data changes occur coincident with the DVAL signal's high-state. The video test pattern data and timing signals from the CLS-212 are automatically replicated (i.e. stalled) for 2/4/8 clock cycles in order to simulate oversampled data coming from cameras that are utilizing the DVAL signal. This is the typical use of DVAL in order to support low pixel clock frequency cameras in Camera Link systems.

See the DVAL and DVAL control register definitions for more information.

1.3.6. Integration Timer

The CLS-212 incorporates an integration timer which may be used to simulate camera exposure characteristics. The integration timer operates off a fixed clock reference and has a range of 0 to 65 seconds in 1ms steps.

The integration timer is used to mimic camera integration (exposure) characteristics by delaying the generation of video frames for a period of time representing the integration interval. The integration timer may be used in conjunction with either continuous or triggered (exsync) mode.

In continuous mode, the integration timer determines the video frame rate and can be set to mimic very long (up-to 65s) integration periods.

In triggered (exsync) mode, the generation of a video frame in response to a triggering event is delayed by the time programmed into the counter in order to mimic an integration interval.

1.3.7. Microcontroller

The CLS-212 Camera Link Simulator utilizes a microcontroller device to implement a Command Line Interface (CLI). The CLI enables a PC to control and monitor CLS-212 functions. The microcontroller interprets commands received over the CLI and configures the CLS-212 circuitry accordingly. The serial communication protocol between the PC/workstation and the CLS-212 is supported by the microcontroller's built-in Universal Asynchronous Receiver/Transmitter (UART).

The microcontroller incorporates non-volatile configuration memory for the storage of user-selected parameters. Upon power-up initialization, the CLS-212 automatically recalls the parameter set stored in memory. This feature enables operation of the CLS-212 without a control port connection. The CLI Parameter Save (SAVE) command is used to store the current parameter set to the configuration memory. The CLI Parameter Recall (RECALL) command configures the CLS-212 using the parameter set currently stored.

1.3.8. RS-232 Serial Port

The CLS-212 Camera Link Simulator incorporates an industry-standard RS-232 serial port for linking the CLS-212 to a host PC. The serial port provides RS-232 signal characteristics and incorporates a standard 9-pin D-Sub (DB9) connector. The serial port protocol settings are conventional and are defined in Table 1-3. Connector information is provided in Section 2.2.

Table 1-3: RS-232 Serial Port Settings

Port Characteristic	Setting
Rate (bits per second)	9600
Data Bits	8
Parity	None
Stop Bits	1
Flow Control	None

1.3.9. USB Support (Optional)

Alternatively, the CLS-212 Camera Link Simulator may be connected to the host computer USB port using an optional external USB to serial RS-232 adapter. This eliminates the problem with using newer desktop and laptop computers that do not incorporate a serial port. One side of the USB to serial adapter plugs into the PC USB port. The other side of the adapter connects to the RS-232 serial cable included with the CLS-212. Once installed, the PC will create a new serial COM port that may be accessed using the PC in the same fashion as the standard RS-232 serial port. Driver software installation may be required.

A USB to serial converter is available from Vivid Engineering for a modest charge. These converters are also available from computer supply retailers.

1.3.10. Camera Control Inputs

The CLS-212 Camera Link Simulator receives four Camera Control (CC1, CC2, CC3, CC4) from the frame grabber as defined in the Camera Link

specification. The camera control signal states can be monitored using the CLI, or used as an exsync input to trigger frame/line output.

CLS-212 can be programmed to select a camera control input (CC1, CC2, CC3, or CC4) for use as an exsync trigger. Exsync trigger polarity (rising or falling edge) is also programmable. When configured, the CLS-212 will issue a single frame (or line in linescan mode) in response to each exsync trigger received.

1.3.11. Channel Link Transmitters

The CLS-212 Camera Link Simulator incorporates Channel Link transmitter devices for outputting video timing, data, and clock in compliance with the Camera Link specification. Three Channel Link transmitter devices are used, one for the "base" connector and two for the "medium/full" connector. High-performance devices are utilized to support the "extended" Camera Link maximum pixel clock frequency of 85 MHz.

The CLS-212 provides the ability to individually disable the channel link transmitter chips. This ceases all activity on the associated Camera Link interface signals and is useful for cable testing and for testing PoCL frame grabber SafePower functionality. See Secttion 1.3.12 for additional information about CLS-212 PoCL features.

The Channel Link transmitter chips are National Semiconductor DS90CR287MTD.

1.3.12. Power over Camera Link (PoCL) Features

The Camera Link Specification includes a version of Camera Link in which power is supplied to the camera via the frame grabber over the Cable Link cable. This is known as Power over Camera Link, abbreviated PoCL. Details of the PoCL scheme including an explanation of the SafePower feature, which safely energizes PoCL cameras, are provided in the Camera Link specification. The following section assumes the reader has a familiarity with Camera Link, PoCL, and SafePower.

Based on the CLS-211 simulator, the CLS-212 adds the following features for testing and exercising Power Over Camera Link (PoCL) interfaces. These features are particularly useful for testing PoCL cables and PoCL frame grabber SafePower functionality:

- Miniature Camera Link (miniCL) connectors
- 10K ohm resistive load
- Power presence detection.
- Clock disable

The CLS-212 Camera Link Simulator incorporates the Miniature Camera Link (miniCL) connector most common used in PoCL cameras. This facilitates testing both the PoCL frame grabber and the PoCL cables used to connect the camera to the frame grabber.

The CLS-212's Camera Link interface includes the 10K ohm resistive load as specified in the Camera Link specification to identify a Camera Link camera. This way, the CLS-212 will appear to be a PoCL camera to frame grabbers that support PoCL. The 10K load is always present. The CLS-212 does not include a provision to disbale the 10K ohm load which would make the CLS-212 appear to be a non-PoCL camera.

The CLS-212 detects the presence of power from the frame grabber. PoCL power presence is available to the host computer via the CLI. Power presence is shown on a front-panel indicator.

The PoCL SafePower scheme used to safely energize cameras monitors clock presence from the camera. If the clock signal from an energized camera disappears, a SafePower PoCL frame grabber will remove power (i.e.

for instances when a SafePower camera is disconnected). The CLS-212 supports exercising/testing this feature by allowing the user to disable each of the three channel link transmitter (i.e. base, medium, full) devices. When a transmitter chip is disabled, the associated clock ceases. See Secttion 1.3.11 for additional information about the CLS-212 Channel Link transmitter devices.

1.4. Command Line Interface (CLI)

The CLS-212 Camera Link Simulator incorporates a Command Line Interface (CLI) which enables CLS-212 control and monitoring using a PC, Mac, workstation, terminal, etc. The CLS-212 requires no special software.

Once the CLS-212 is connected to a host computer RS-232 port (or USB port using the optional adapter), the user accesses the CLS-212 using standard communications software. HyperTerminal included in the Windows software works well as does almost any basic communications software package. By default, the CLS-212 echoes-back all characters received. The Echo Control (ECHO) command enables the user to enable/disable echo. Disabling echo is sometimes desired, in particular when large configuration files are being downloaded to the CLS-212. Serial port settings are listed in Section 1.3.7.

HyperTerminal Note:

The CLS-212 serial port interface does not incorporate flow control. While data buffering is performed, it is still possible to overrun the CLS-212 receive buffer, especially when downloading large configuration files. This will be visible as lost characters on the console and/or "invalid entry" responses from the CLS-212. The following methods may be used to avoid these problems:

1. Turn off message echo when downloading large configuration files. Turning of echo is performed via the Echo Control (ECHO) command.

2. In HyperTerminal , click on the *Files* menu. Then click on *Properties* - *Settings* - *ASCII Setup* - and enter a "1" for the *character delay* and/or the *line delay*.

Upon power-up, the CLS-212 performs system initialization and will respond with a message similar to the following:

```
CLS-212 initializing, please wait
. . . . . .
ready
```

Following initialization, the CLS-212 then sends the PC a message similar to the following:

```
CLS212 Camera Link Simulator CLI
Vivid Engineering
Rev 1.00
```

The CLS-212 recognizes the commands defined in the following sections. The DUMP, SAVE, and RECALL commands are particularly useful. In the case of invalid syntax, the CLS-212 responds with the following:

```
invalid entry
```

All numeric entries are made using <u>either</u> decimal or hexadecimal (0x…) notation. The only exception is the long Clock Synthesizer Code (SYNTH_CODE) command which is always entered as hexadecimal.

CLS-212 parameters may be entered manually on the keyboard, or may be downloaded to the CLS-212 as a configuration file. Configuration files are plain text format (i.e. "*.txt"* files) and may be created with an editor, word processor, etc. Spaces and returns may be inserted as desired for readability. Comments are indicated using a backslash "/" and may be located at the start of a line or following a command. The following is an example of comments located in a configuration file. Note that all numeric information must be in either decimal or hexadecimal (0x…) format. An example configuration file is found in Section 1-5.

```
//   Camera Link Configuration File
//   - syntax example
LVAL_LO     0x0020      // hexadecimal notation
LVAL_HI     500         // decimal notation
Fval_lo     0x20        // hexadecimal notation
```

Methods for downloading text (.txt) files to the CLS-212 vary depending on the communications software used. For HyperTerminal (included with Windows), click on the "Transfer" toolbar and select "Send Text File". HyperTerminal will then prompt for the location of the file.

The CLS-212 command set is defined in the following sections.

1.4.1. Line Valid Low (LVAL_LO)

The Line Valid Low (LVAL_LO) command is used to establish the duration, in clock cycles for the "low" (logic 0) portion of the Camera Link Line Valid timing signal. See Section 1.3.2 for further information.

Parameter: LVAL_LO
Range: 1-65535 clocks *(hex 0x1 - 0xFFFF)*
Type: Read/Write

Write Example: **LVAL_LO 0xA000**
Read Example: **LVAL_LO ?**

1.4.2. Line Valid High (LVAL_HI)

The Line Valid High (LVAL_HI) command is used to establish the duration, in clock cycles for the "high" (logic 1) portion of the Camera Link Line Valid timing signal. See Section 1.3.2 for further information.

Parameter: LVAL_HI
Range: 1-65535 clocks *(hex 0x1 - 0xFFFF)*
Type: Read/Write

Write Example: **LVAL_HI 0xB000**
Read Example: **LVAL_HI ?**

1.4.3. Frame Valid Low (FVAL_LO)

The Frame Valid Low (FVAL_LO) command is used to establish the duration, in lines for the "low" (logic 0) portion of the Camera Link Frame Valid timing signal. See Section 1.3.2 for further information.

Parameter: FVAL_LO
Range: 1-65535 lines *(hex 0x1 - 0xFFFF)*
Type: Read/Write

Write Example: **FVAL_LO 0xC000**
Read Example: **FVAL_LO ?**

1.4.4. Frame Valid High (FVAL_HI)

The Frame Valid High (FVAL_HI) command is used to establish the duration, in lines for the "high" (logic 1) portion of the Camera Link Frame Valid timing signal. See Section 1.3.2 for further information.

Parameter: FVAL_HI
Range: 1-65535 lines *(hex 0x1 - 0xFFFF)*
Type: Read/Write

Write Example: **FVAL_HI 0xD000**
Read Example: **FVAL_HI ?**

1.4.5. Frame Valid Setup (FVAL_SETUP)

The Frame Valid Setup (FVAL_SETUP) command determines the number of clock cycles that the rising edge of the Camera Link FVAL signal occurs in advance of the falling edge of the LVAL signal. When FVAL_SETUP is set to 0, the rising edge of FVAL is coincident with the falling edge of LVAL. See Section 1.3.2 for further information.

Parameter: FVAL_SETUP
Range: 0-65535 clocks *(hex 0x0 - 0xFFFF)*
Type: Read/Write

Write Example: **FVAL_SETUP 0xE000**
Read Example: **FVAL_SETUP ?**

1.4.6. Frame Valid Hold (FVAL_HOLD)

The Frame Valid Hold (FVAL_HOLD) command determines the number of clock cycles that the falling edge of the Camera Link FVAL signal occurs following the falling edge of the LVAL signal. When FVAL_HOLD is set to 0, the falling edge of FVAL is coincident with the falling edge of LVAL. See Section 1.3.2 for further information.

Parameter: FVAL_HOLD
Range: 0-65535 clocks *(hex 0x0 - 0xFFFF)*
Type: Read/Write

Write Example: **FVAL_HOLD 0x1000**
Read Example: **FVAL_HOLD ?**

1.4.7. X Offset (X_OFFSET)

The X Offset (X_OFFSET) command determines the number of clock cycles from the rising edge of the Camera Link LVAL signal to the start of test pattern data (i.e. horizontal start position). When X_OFFSET is set to 0, line test pattern data begins immediately following the rising edge of LVAL. See Section 1.3.3 for further information.

Parameter: X_OFFSET
Range: 0-65535 clocks *(hex 0x0 - 0xFFFF)*
Type: Read/Write

Write Example: **X_OFFSET 0x2000**
Read Example: **X_OFFSET ?**

1.4.8. X Active (X_ACTIVE)

The X Active (X_ACTIVE) command determines the horizontal size (x dimension) of the test pattern in clock cycles. See Section 1.3.3 for further information.

Parameter: X_ACTIVE
Range: 1-65535 clocks *(hex 0x1 - 0xFFFF)*
Type: Read/Write

Write Example: **X_ACTIVE 0x3000**
Read Example: **X_ACTIVE ?**

1.4.9. Y Offset (Y_OFFSET)

The Y Offset (Y_OFFSET) command determines the number of lines from the rising edge of the Camera Link FVAL signal to the start of test pattern data (i.e. vertical start position). When Y_OFFSET is set to 0, the test pattern data begins with the next line. See Section 1.3.3 for further information.

Parameter: Y_OFFSET
Range: 0-65535 clocks *(hex 0x0 - 0xFFFF)*
Type: Read/Write

Write Example: **Y_OFFSET 0x4000**
Read Example: **Y_OFFSET ?**

1.4.10. Y Active (Y_ACTIVE)

The Y Active (Y_ACTIVE) command determines the vertical size (y dimension) of the test pattern in lines. See Section 1.3.3 for further information.

Parameter: Y_ACTIVE
Range: 1-65535 lines *(hex 0x1 - 0xFFFF)*
Type: Read/Write

Write Example: **Y_ACTIVE 0x5000**
Read Example: **Y_ACTIVE ?**

1.4.11. Pixel "A" Pattern Select (A_PATSEL)

The Pixel "A" Pattern Select (A_PATSEL) command assigns the test pattern for video data pixel "A". The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: A_PATSEL
Settings: 0x0 = Fixed Value
0x1 = Horizontal Wedge
0x2 = Vertical Wedge
0x3 = Diagonal Wedge
Type: Read/Write

Write Example: **A_PATSEL 0x0**
Read Example: **A_PATSEL ?**

1.4.12. Pixel "B" Pattern Select (B_PATSEL)

The Pixel "B" Pattern Select (B_PATSEL) command assigns the test pattern for video data pixel "B". The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: B_PATSEL
Settings: 0 (0x0) = Fixed Value
1 (0x1) = Horizontal Wedge
2 (0x2) = Vertical Wedge
3 (0x3) = Diagonal Wedge
Type: Read/Write

Write Example: **B_PATSEL 0x2**
Read Example: **B_PATSEL ?**

1.4.13. Pixel "C" Pattern Select (C_PATSEL)

The Pixel "C" Pattern Select (C_PATSEL) command assigns the test pattern for video data pixel "C". The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: C_PATSEL
Settings: 0 (0x0) = Fixed Value
1 (0x1) = Horizontal Wedge
2 (0x2) = Vertical Wedge
3 (0x3) = Diagonal Wedge
Type: Read/Write

Write Example: **C_PATSEL 0x2**
Read Example: **C_PATSEL ?**

1.4.14. Pixel "D" Pattern Select (D_PATSEL)

The Pixel "D" Pattern Select (D_PATSEL) command assigns the test pattern for video data pixel "D". The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: D_PATSEL
Settings: 0 (0x0) = Fixed Value
1 (0x1) = Horizontal Wedge
2 (0x2) = Vertical Wedge
3 (0x3) = Diagonal Wedge
Type: Read/Write

Write Example: **D_PATSEL 0x3**
Read Example: **D_PATSEL ?**

1.4.15. Pixel "E" Pattern Select (E_PATSEL)

The Pixel "E" Pattern Select (E_PATSEL) command assigns the test pattern for video data pixel "E". The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: E_PATSEL
Settings: 0 (0x0) = Fixed Value
1 (0x1) = Horizontal Wedge

2 (0x2) = Vertical Wedge
3 (0x3) = Diagonal Wedge
Type: Read/Write

Write Example: **E_PATSEL 0x3**
Read Example: **E_PATSEL ?**

1.4.16. Pixel "F" Pattern Select (F_PATSEL)

The Pixel "F" Pattern Select (F_PATSEL) command assigns the test pattern for video data pixel "F". The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: F_PATSEL
Settings: 0 (0x0) = Fixed Value
1 (0x1) = Horizontal Wedge
2 (0x2) = Vertical Wedge
3 (0x3) = Diagonal Wedge
Type: Read/Write

Write Example: **F_PATSEL 0x3**
Read Example: **F_PATSEL ?**

1.4.17. Pixel "G" Pattern Select (G_PATSEL)

The Pixel "G" Pattern Select (G_PATSEL) command assigns the test pattern for video data pixel "G". The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: G_PATSEL
Settings: 0 (0x0) = Fixed Value
1 (0x1) = Horizontal Wedge
2 (0x2) = Vertical Wedge
3 (0x3) = Diagonal Wedge
Type: Read/Write

Write Example: **G_PATSEL 0x3**
Read Example: **G_PATSEL ?**

1.4.18. Pixel "H" Pattern Select (H_PATSEL)

The Pixel "H" Pattern Select (H_PATSEL) command assigns the test pattern for video data pixel "H". The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: H_PATSEL
Settings: 0 (0x0) = Fixed Value
1 (0x1) = Horizontal Wedge
2 (0x2) = Vertical Wedge
3 (0x3) = Diagonal Wedge
Type: Read/Write

Write Example: **H_PATSEL 0x3**
Read Example: **H_PATSEL ?**

1.4.19. Pixel "I" Pattern Select (I_PATSEL)

The Pixel "I" Pattern Select (I_PATSEL) command assigns the test pattern for video data pixel "I". The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: I_PATSEL
Settings: 0 (0x0) = Fixed Value
1 (0x1) = Horizontal Wedge
2 (0x2) = Vertical Wedge
3 (0x3) = Diagonal Wedge
Type: Read/Write

Write Example: **I_PATSEL 0x3**
Read Example: **I_PATSEL ?**

1.4.20. Pixel "J" Pattern Select (J_PATSEL)

The Pixel "J" Pattern Select (J_PATSEL) command assigns the test pattern for video data pixel "J". The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: J_PATSEL
Settings: 0 (0x0) = Fixed Value
1 (0x1) = Horizontal Wedge

2 (0x2) = Vertical Wedge
3 (0x3) = Diagonal Wedge

Type: Read/Write

Write Example: **J_PATSEL 0x3**
Read Example: **J_PATSEL ?**

1.4.21. Pixel "A" Fixed Value (A_FIXED)

The Pixel "A" Fixed Value (A_FIXED) command determines the pixel "A" value when the fixed pattern is selected (A_PATSEL = 0). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: A_FIXED
Range: Depends on pixel size. 0-65535 *(hex 0x0 - 0xFFFF)* max.
Type: Read/Write

Write Example: **A_FIXED 0xA5A5**
Read Example: **A_FIXED ?**

1.4.22. Pixel "B" Fixed Value (B_FIXED)

The Pixel "B" Fixed Value (B_FIXED) command determines the pixel "B" value when the fixed pattern is selected (B_PATSEL = 0). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: B_FIXED
Range: Depends on pixel size. 0-4095 *(hex 0x0 - 0xFFF)* max.
Type: Read/Write

Write Example: **B_FIXED 0x5A5**
Read Example: **B_FIXED ?**

1.4.23. Pixel "C" Fixed Value (C_FIXED)

The Pixel "C" Fixed Value (C_FIXED) command determines the pixel "C" value when the fixed pattern is selected (C_PATSEL = 0). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: C_FIXED
Range: Depends on pixel size. 0-4095 *(hex 0x0 - 0xFFF)* max.
Type: Read/Write

Write Example: **C_FIXED 0x3C3**
Read Example: **C_FIXED ?**

1.4.24. Pixel "D" Fixed Value (D_FIXED)

The Pixel "D" Fixed Value (D_FIXED) command determines the pixel "D" value when the fixed pattern is selected (D_PATSEL = 0). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: D_FIXED
Range: Depends on pixel size. 0-4095 *(hex 0x0 - 0xFFF)* max.
Type: Read/Write

Write Example: **D_FIXED 0xC3C**
Read Example: **D_FIXED ?**

1.4.25. Pixel "E" Fixed Value (E_FIXED)

The Pixel "E" Fixed Value (E_FIXED) command determines the pixel "E" value when the fixed pattern is selected (E_PATSEL = 0). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: E_FIXED
Range: Depends on pixel size. 0-1023 *(hex 0x0 - 0x3FF)* max.
Type: Read/Write

Write Example: **E_FIXED 0x23C**
Read Example: **E_FIXED ?**

1.4.26. Pixel "F" Fixed Value (F_FIXED)

The Pixel "F" Fixed Value (F_FIXED) command determines the pixel "F" value when the fixed pattern is selected (F_PATSEL = 0). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: F_FIXED
Range: Depends on pixel size. 0-1023 *(hex 0x0 - 0x3FF)* max.
Type: Read/Write

Write Example: **F_FIXED 0x23C**
Read Example: **F_FIXED ?**

1.4.27. Pixel "G" Fixed Value (G_FIXED)

The Pixel "G" Fixed Value (G_FIXED) command determines the pixel "G" value when the fixed pattern is selected (G_PATSEL = 0). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: G_FIXED
Range: Depends on pixel size. 0-1023 *(hex 0x0 - 0x3FF)* max.
Type: Read/Write

Write Example: **G_FIXED 0x23C**
Read Example: **G_FIXED ?**

1.4.28. Pixel "H" Fixed Value (H_FIXED)

The Pixel "H" Fixed Value (H_FIXED) command determines the pixel "H" value when the fixed pattern is selected (H_PATSEL = 0). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: H_FIXED
Range: Depends on pixel size. 0-1023 *(hex 0x0 - 0x3FF)* max.
Type: Read/Write

Write Example: **H_FIXED 0x23C**
Read Example: **H_FIXED ?**

1.4.29. Pixel "I" Fixed Value (I_FIXED)

The Pixel "I" Fixed Value (I_FIXED) command determines the pixel "I" value when the fixed pattern is selected (I_PATSEL = 0). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: I_FIXED
Range: 0-255 *(hex 0x0 - 0xFF)*
Type: Read/Write

Write Example: **I_FIXED 0x3C**
Read Example: **I_FIXED ?**

1.4.30. Pixel "J" Fixed Value (J_FIXED)

The Pixel "J" Fixed Value (J_FIXED) command determines the pixel "J" value when the fixed pattern is selected (J_PATSEL = 0). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: J_FIXED
Range: 0-255 *(hex 0x0 - 0xFF)*
Type: Read/Write

Write Example: **J_FIXED 0x3C**
Read Example: **J_FIXED ?**

1.4.31. Pixel "A" Background Value (A_BACK)

The Pixel "A" Background Value (A_BACK) command determines the default value for video data pixel "A". The default value is output whenever the CLS-212 is not outputting video test pattern data. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: A_BACK
Range: Depends on pixel size. 0-65535 *(hex 0x0 - 0xFFFF)* max.
Type: Read/Write

Write Example: **A_BACK 0xA5A5**
Read Example: **A_BACK ?**

1.4.32. Pixel "B" Background Value (B_BACK)

The Pixel "B" Background Value (B_BACK) command determines the default value for video data pixel "B". The default value is output whenever the CLS-212 is not outputting video test pattern data. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Range: Depends on pixel size. 0-4095 *(hex 0x0 - 0xFFF)* max.
Type: Read/Write

Write Example: **B_BACK 0x5A5**
Read Example: **B_BACK ?**

1.4.33. Pixel "C" Background Value (C_BACK)

The Pixel "C" Background Value (C_BACK) command determines the default value for video data pixel "C". The default value is output whenever the CLS-212 is not outputting video test pattern data. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: C_BACK
Range: Depends on pixel size. 0-4095 *(hex 0x0 - 0xFFF)* max.
Type: Read/Write

Write Example: **C_BACK 0xC3C**
Read Example: **C_BACK ?**

1.4.34. Pixel "D" Background Value (D_BACK)

The Pixel "D" Background Value (D_BACK) command determines the default value for video data pixel "D". The default value is output whenever the CLS-212 is not outputting video test pattern data. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: D_BACK
Range: Depends on pixel size. 0-4095 *(hex 0x0 - 0xFFF)* max.
Type: Read/Write

Write Example: **D_BACK 0x3C3**
Read Example: **D_BACK ?**

1.4.35. Pixel "E" Background Value (E_BACK)

The Pixel "E" Background Value (E_BACK) command determines the default value for video data pixel "E". The default value is output whenever the CLS-212 is not outputting video test pattern data. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: E_BACK
Range: Depends on pixel size. 0-1023 *(hex 0x0 - 0x3FF)* max.
Type: Read/Write

Write Example: **E_BACK 0x2C3**
Read Example: **E_BACK ?**

1.4.36. Pixel "F" Background Value (F_BACK)

The Pixel "F" Background Value (F_BACK) command determines the default value for video data pixel "F". The default value is output whenever the CLS-212 is not outputting video test pattern data. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: F_BACK
Range: Depends on pixel size. 0-1023 *(hex 0x0 - 0x3FF)* max.
Type: Read/Write

Write Example: **F_BACK 0x2C3**
Read Example: **F_BACK ?**

1.4.37. Pixel "G" Background Value (G_BACK)

The Pixel "G" Background Value (G_BACK) command determines the default value for video data pixel "G". The default value is output whenever the CLS-212 is not outputting video test pattern data. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: G_BACK
Range: Depends on pixel size. 0-1023 *(hex 0x0 - 0x3FF)* max.
Type: Read/Write

Write Example: **G_BACK 0x2C3**
Read Example: **G_BACK ?**

1.4.38. Pixel "H" Background Value (H_BACK)

The Pixel "H" Background Value (H_BACK) command determines the default value for video data pixel "H". The default value is output whenever the CLS-212 is not outputting video test pattern data. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: H_BACK
Range: Depends on pixel size. 0-1023 *(hex 0x0 - 0x3FF)* max.
Type: Read/Write

Write Example: **H_BACK 0x2C3**
Read Example: **H_BACK ?**

1.4.39. Pixel "I" Background Value (I_BACK)

The Pixel "I" Background Value (I_BACK) command determines the default value for video data pixel "I". The default value is output whenever the CLS-212 is not outputting video test pattern data. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: I_BACK
Range: 0-255 *(hex 0x0 - 0xFF)*
Type: Read/Write

Write Example: **I_BACK 0xC3**
Read Example: **I_BACK ?**

1.4.40. Pixel "J" Background Value (J_BACK)

The Pixel "J" Background Value (J_BACK) command determines the default value for video data pixel "J". The default value is output whenever the CLS-212 is not outputting video test pattern data. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: J_BACK
Range: 0-255 *(hex 0x0 - 0xFF)*
Type: Read/Write

Write Example: **J_BACK 0xC3**
Read Example: **J_BACK ?**

1.4.41. Pixel "A" Pattern Step (A_STEP)

The Pixel "A" Pattern Step (A_STEP) command determines the amount by which the "A" pixel value increments in the wedge (horizontal, vertical, diagonal) video test patterns. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter:	A_STEP
Settings:	1 (0x1) = Increment by 1 (0,1,2…)
	2 (0x2) = Increment by 2 (0,2,4…)
	4 (0x2) = Increment by 4 (0,4,8…)
	8 (0x8) = Increment by 8 (0,8,16…)
	16 (0x10) = Increment by 16 (0,16,32…)
	32 (0x20) = Increment by 32 (0,32,64…)
	64 (0x40) = Increment by 64 (0,64,128…)
	128 (0x80) = Increment by 128 (0,128,256…)
Type:	Read/Write

Write Example: **A_STEP 0x2**
Read Example: **A_STEP ?**

1.4.42. Pixel "B" Pattern Step (B_STEP)

The Pixel "B" Pattern Step (B_STEP) command determines the amount by which the "B" pixel value increments in the wedge (horizontal, vertical, diagonal) video test patterns. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter:	B_STEP
Settings:	1 (0x1) = Increment by 1 (0,1,2…)
	2 (0x2) = Increment by 2 (0,2,4…)
	4 (0x2) = Increment by 4 (0,4,8…)
	8 (0x8) = Increment by 8 (0,8,16…)
	16 (0x10) = Increment by 16 (0,16,32…)
	32 (0x20) = Increment by 32 (0,32,64…)
	64 (0x40) = Increment by 64 (0,64,128…)
	128 (0x80) = Increment by 128 (0,128,256…)
Type:	Read/Write

Write Example: **B_STEP 0x2**
Read Example: **B_STEP ?**

1.4.43. Pixel "C" Pattern Step (C_STEP)

The Pixel "C" Pattern Step (C_STEP) command determines the amount by which the "C" pixel value increments in the wedge (horizontal, vertical, diagonal) video test patterns. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter:	C_STEP
Settings:	1 (0x1) = Increment by 1 (0,1,2…)
	2 (0x2) = Increment by 2 (0,2,4…)
	4 (0x2) = Increment by 4 (0,4,8…)
	8 (0x8) = Increment by 8 (0,8,16…)
	16 (0x10) = Increment by 16 (0,16,32…)
	32 (0x20) = Increment by 32 (0,32,64…)
	64 (0x40) = Increment by 64 (0,64,128…)
	128 (0x80) = Increment by 128 (0,128,256…)
Type:	Read/Write

Write Example: **C_STEP 0x2**
Read Example: **C_STEP ?**

1.4.44. Pixel "D" Pattern Step (D_STEP)

The Pixel "D" Pattern Step (D_STEP) command determines the amount by which the "D" pixel value increments in the wedge (horizontal, vertical, diagonal) video test patterns. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter:	D_STEP
Settings:	1 (0x1) = Increment by 1 (0,1,2…)
	2 (0x2) = Increment by 2 (0,2,4…)
	4 (0x2) = Increment by 4 (0,4,8…)
	8 (0x8) = Increment by 8 (0,8,16…)
	16 (0x10) = Increment by 16 (0,16,32…)
	32 (0x20) = Increment by 32 (0,32,64…)
	64 (0x40) = Increment by 64 (0,64,128…)
	128 (0x80) = Increment by 128 (0,128,256…)
Type:	Read/Write

Write Example: **D_STEP 0x2**
Read Example: **D_STEP ?**

1.4.45. Pixel "E" Pattern Step (E_STEP)

The Pixel "E" Pattern Step (E_STEP) command determines the amount by which the "E" pixel value increments in the wedge (horizontal, vertical, diagonal) video test patterns. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter:	E_STEP
Settings:	1 (0x1) = Increment by 1 (0,1,2…)
	2 (0x2) = Increment by 2 (0,2,4…)
	4 (0x2) = Increment by 4 (0,4,8…)
	8 (0x8) = Increment by 8 (0,8,16…)
	16 (0x10) = Increment by 16 (0,16,32…)
	32 (0x20) = Increment by 32 (0,32,64…)
	64 (0x40) = Increment by 64 (0,64,128…)
	128 (0x80) = Increment by 128 (0,128,256…)
Type:	Read/Write

Write Example: **E_STEP 0x2**
Read Example: **E_STEP ?**

1.4.46. Pixel "F" Pattern Step (F_STEP)

The Pixel "F" Pattern Step (F_STEP) command determines the amount by which the "F" pixel value increments in the wedge (horizontal, vertical, diagonal) video test patterns. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter:	F_STEP
Settings:	1 (0x1) = Increment by 1 (0,1,2…)
	2 (0x2) = Increment by 2 (0,2,4…)
	4 (0x2) = Increment by 4 (0,4,8…)
	8 (0x8) = Increment by 8 (0,8,16…)
	16 (0x10) = Increment by 16 (0,16,32…)
	32 (0x20) = Increment by 32 (0,32,64…)
	64 (0x40) = Increment by 64 (0,64,128…)
	128 (0x80) = Increment by 128 (0,128,256…)
Type:	Read/Write

Write Example: **F_STEP 0x2**
Read Example: **F_STEP ?**

1.4.47. Pixel "G" Pattern Step (G_STEP)

The Pixel "G" Pattern Step (G_STEP) command determines the amount by which the "G" pixel value increments in the wedge (horizontal, vertical, diagonal) video test patterns. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter:	G_STEP
Settings:	1 (0x1) = Increment by 1 (0,1,2…)
	2 (0x2) = Increment by 2 (0,2,4…)
	4 (0x2) = Increment by 4 (0,4,8…)
	8 (0x8) = Increment by 8 (0,8,16…)
	16 (0x10) = Increment by 16 (0,16,32…)
	32 (0x20) = Increment by 32 (0,32,64…)
	64 (0x40) = Increment by 64 (0,64,128…)
	128 (0x80) = Increment by 128 (0,128,256…)
Type:	Read/Write

Write Example: **G_STEP 0x2**
Read Example: **G_STEP ?**

1.4.48. Pixel "H" Pattern Step (H_STEP)

The Pixel "H" Pattern Step (H_STEP) command determines the amount by which the "H" pixel value increments in the wedge (horizontal, vertical, diagonal) video test patterns. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter:	H_STEP
Settings:	1 (0x1) = Increment by 1 (0,1,2…)
	2 (0x2) = Increment by 2 (0,2,4…)
	4 (0x2) = Increment by 4 (0,4,8…)
	8 (0x8) = Increment by 8 (0,8,16…)
	16 (0x10) = Increment by 16 (0,16,32…)
	32 (0x20) = Increment by 32 (0,32,64…)
	64 (0x40) = Increment by 64 (0,64,128…)
	128 (0x80) = Increment by 128 (0,128,256…)
Type:	Read/Write

Write Example: **H_STEP 0x2**
Read Example: **H_STEP ?**

1.4.49. Pixel "I" Pattern Step (I_STEP)

The Pixel "I" Pattern Step (I_STEP) command determines the amount by which the "I" pixel value increments in the wedge (horizontal, vertical, diagonal) video test patterns. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter:	I_STEP
Settings:	1 (0x1) = Increment by 1 (0,1,2…)
	2 (0x2) = Increment by 2 (0,2,4…)
	4 (0x2) = Increment by 4 (0,4,8…)
	8 (0x8) = Increment by 8 (0,8,16…)
	16 (0x10) = Increment by 16 (0,16,32…)
	32 (0x20) = Increment by 32 (0,32,64…)
	64 (0x40) = Increment by 64 (0,64,128…)
	128 (0x80) = Increment by 128 (0,128,256…)
Type:	Read/Write

Write Example: **I_STEP 0x2**
Read Example: **I_STEP ?**

1.4.50. Pixel "J" Pattern Step (J_STEP)

The Pixel "J" Pattern Step (J_STEP) command determines the amount by which the "J" pixel value increments in the wedge (horizontal, vertical, diagonal) video test patterns. The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter:	J_STEP
Settings:	1 (0x1) = Increment by 1 (0,1,2…)
	2 (0x2) = Increment by 2 (0,2,4…)
	4 (0x2) = Increment by 4 (0,4,8…)
	8 (0x8) = Increment by 8 (0,8,16…)
	16 (0x10) = Increment by 16 (0,16,32…)
	32 (0x20) = Increment by 32 (0,32,64…)
	64 (0x40) = Increment by 64 (0,64,128…)
	128 (0x80) = Increment by 128 (0,128,256…)
Type:	Read/Write

Write Example: **J_STEP 0x2**
Read Example: **J_STEP ?**

1.4.51. Pixel "A" Init Value (A_INIT)

The Pixel "A" Init Value (A_INIT) command determines the initial value of pixel "A" when one of the wedge patterns is selected (A_PATSEL = 1-3). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: A_INIT
Range: Depends on pixel size. 0-65535 *(hex 0x0 - 0xFFFF)* max.
Type: Read/Write

Write Example: **A_INIT 0xA5A5**
Read Example: **A_INIT ?**

1.4.52. Pixel "B" Init Value (B_INIT)

The Pixel "B" Init Value (B_INIT) command determines the initial value of pixel "B" when one of the wedge patterns is selected (B_PATSEL = 1-3). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: B_INIT
Range: Depends on pixel size. 0-4095 *(hex 0x0 - 0xFFF)* max.
Type: Read/Write

Write Example: **B_INIT 0x5A5**
Read Example: **B_INIT ?**

1.4.53. Pixel "C" Init Value (C_INIT)

The Pixel "C" Init Value (C_INIT) command determines the initial value of pixel "C" when one of the wedge patterns is selected (C_PATSEL = 1-3). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: C_INIT
Range: Depends on pixel size. 0-4095 *(hex 0x0 - 0xFFF)* max.
Type: Read/Write

Write Example: **C_INIT 0x3C3**
Read Example: **C_INIT ?**

1.4.54. Pixel "D" Init Value (D_INIT)

The Pixel "D" Init Value (D_INIT) command determines the initial value of pixel "D" when one of the wedge patterns is selected (D_PATSEL = 1-3). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: D_INIT
Range: Depends on pixel size. 0-4095 *(hex 0x0 - 0xFFF)* max.
Type: Read/Write

Write Example: **D_INIT 0xC3C**
Read Example: **D_INIT ?**

1.4.55. Pixel "E" Init Value (E_INIT)

The Pixel "E" Init Value (E_INIT) command determines the initial value of pixel "E" when one of the wedge patterns is selected (E_PATSEL = 1-3). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: E_INIT
Range: Depends on pixel size. 0-1023 *(hex 0x0 - 0x3FF)* max.
Type: Read/Write

Write Example: **E_INIT 0x23C**
Read Example: **E_INIT ?**

1.4.56. Pixel "F" Init Value (F_INIT)

The Pixel "F" Init Value (F_INIT) command determines the initial value of pixel "F" when one of the wedge patterns is selected (F_PATSEL = 1-3). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: F_INIT
Range: Depends on pixel size. 0-1023 *(hex 0x0 - 0x3FF)* max.
Type: Read/Write

Write Example: **F_INIT 0x23C**
Read Example: **F_INIT ?**

1.4.57. Pixel "G" Init Value (G_INIT)

The Pixel "G" Init Value (G_INIT) command determines the initial value of pixel "G" when one of the wedge patterns is selected (G_PATSEL = 1-3). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: G_INIT
Range: Depends on pixel size. 0-1023 *(hex 0x0 - 0x3FF)* max.
Type: Read/Write

Write Example: **G_INIT 0x23C**
Read Example: **G_INIT ?**

1.4.58. Pixel "H" Init Value (H_INIT)

The Pixel "H" Init Value (H_INIT) command determines the initial value of pixel "H" when one of the wedge patterns is selected (H_PATSEL = 1-3). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: H_INIT
Range: Depends on pixel size. 0-1023 *(hex 0x0 - 0x3FF)* max.
Type: Read/Write

Write Example: **H_INIT 0x23C**
Read Example: **H_INIT ?**

1.4.59. Pixel "I" Init Value (I_INIT)

The Pixel "I" Init Value (I_INIT) command determines the initial value of pixel "I" when one of the wedge patterns is selected (I_PATSEL = 1-3). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: I_INIT
Range: 0-255 *(hex 0x0 - 0xFF)*
Type: Read/Write

Write Example: **I_INIT 0x3C**
Read Example: **I_INIT ?**

1.4.60. Pixel "J" Init Value (J_INIT)

The Pixel "J" Init Value (J_INIT) command determines the initial value of pixel "J" when one of the wedge patterns is selected (J_PATSEL = 1-3). The CLS-212 outputs up-to ten pixels simultaneously (A,B,C,D,E,F,G,H,I,J), depending on output mode (see CL_MODE command). See Section 1.3.4 for further information.

Parameter: J_INIT
Range: 0-255 *(hex 0x0 - 0xFF)*
Type: Read/Write

Write Example: **J_INIT 0x3C**
Read Example: **J_INIT ?**

1.4.61. Camera Link Mode (CL_MODE)

The Camera Link Mode (CL_MODE) command determines the test pattern pixel format. The CLS-212 generates video test patterns for all Camera Link modes supported by the Camera Link "base", "medium", and "full" configurations. The CLS-212 also supports both 80-bit configurations. See Section 1.3.4 for further information.

Parameter:	CL_MODE
Settings:	0 (0x0) = 8-bit x 1~3 (base config)
	1 (0x1) = 10-bit x 1~2 (base config)
	2 (0x2) = 12-bit x 1~2 (base config)
	3 (0x3) = 14-bit x 1 (base config)
	4 (0x4) = 16-bit x 1 (base config)
	5 (0x5) = 24-bit RGB (base config)
	8 (0x8) = 8-bit x 4 (medium config)
	9 (0x9) = 10-bit x 3~4 (medium config)
	10 (0xA) = 12-bit x 3~4 (medium config)
	11 (0xB) = 30-bit RGB (medium config)
	12 (0xC) = 36-bit RGB (medium config)
	13 (0xD) = 8-bit x 10 (Deca config)
	14 (0xE) = 10-bit x 8 (full config, 10-bit)
	15 (0xF) = 8-bit x 8 (full config)
Type:	Read/Write

Write Example: **CL_MODE 0x2**
Read Example: **CL_MODE ?**

1.4.62. Pattern Roll (ROLL)

The Pattern Roll (ROLL) command adds motion to video test patterns. Roll is used in conjunction with the horizontal, diagonal, or vertical wedge patterns. When ROLL is enabled, the starting pixel value is incremented every frame. This changes all pixel values each frame and adds a "rolling" affect to the video test pattern. When disabled, the wedge test patterns are static (no change from frame to frame). See Section 1.3.4 for further information.

Parameter:	ROLL
Settings:	0 (0x0) = Roll disable
	1 (0x1) = Roll enabled
Type:	Read/Write

Write Example: **ROLL 0x1**
Read Example: **ROLL ?**

1.4.63. Clock Synthesizer Code (SYNTH_CODE)

The Clock Synthesizer Code (SYNTH_CODE) command enables the user to directly enter a 24-bit code into the clock synthesizer device that generates the CLS-212 reference clock. This allows the user to program the reference clock to virtually any frequency in the 20-85 MHz extended Camera Link range. Two commands are provided in the CLS-212 to establish pixel clock frequency; SYNTH_CODE and FREQUENCY. SYNTH_CODE provides maximum flexibility by allowing direct entry of the 24-bit synthesizer code. FREQUENCY provides convenience by allowing the user to select any integer frequency value between 20 and 85. The most –recent SYNTH_CODE or FREQUENCY command determines the frequency. Reads of the clock command not used returns "####". Reads of the clock command used return a value. See Section 1.3.1 for further information.

NOTE: MUST BE ENTERRED IN HEXADECIMAL (0x…) NOTATION.

Parameter: SYNTH_CODE
Settings: 24-bit Synthesizer Device Code (Hex)
Type: Read/Write

Write Example: **SYNTH_CODE 0x33543D**
Read Example: **SYNTH_CODE ?**

1.4.64. Clock Frequency (FREQUENCY)

The Clock Frequency (FREQUENCY) command enables the user to select integer values for the Camera Link reference clock in the 20-85 MHz range. Two commands are provided in the CLS-212 to establish pixel clock frequency; SYNTH_CODE and FREQUENCY. SYNTH_CODE provides maximum flexibility by allowing direct entry of the 24-bit synthesizer code. FREQUENCY provides convenience by allowing the user to select any integer frequency value between 20 and 85. The most –recent SYNTH_CODE or FREQUENCY command determines the frequency. Reads of the clock command not used returns "####". Reads of the clock command used return a value. See Section 1.3.1 for further information.

Parameter: FREQUENCY
Range: 20-85 MHz *(hex 0x14 - 0x55)*
Type: Read/Write

Write Example: **FREQUENCY 0x14**
Read Example: **FREQUENCY ?**

1.4.65. Continuous Mode (CONTINUOUS)

The Continuous Mode (CONTINUOUS) command enables continuous output of video test patterns. When continuous mode is enabled, the CLS-212 outputs continuous video data. When disabled, video pattern data is suspended, awaiting an exsync pulse, one-shot, or return to continuous mode. See Section 1.3.2 for further information.

Parameter: CONTINUOUS
Settings: 0 (0x0) = Continuous Mode Disabled
1 (0x1) = Continuous Mode Enabled
Type: Read/Write

Write Example: **CONTINUOUS 0x1**
Read Example: **CONTINUOUS ?**

1.4.66. Exsync Enable (EXSYNC_ENB)

The Exsync Enable (EXSYNC_ENB) command enables triggered output of pattern frames (or lines in LINESCAN mode) using the camera control inputs (CC1, CC2, CC3, CC4). The exsync camera control input source and active edge are selected using the EXSYNC_SEL command. See Section 1.3.8 for further information.

Parameter: EXSYNC_ENB
Settings: 0 (0x0) = Exsync Triggering Disabled
1 (0x1) = Exsync Triggering Enabled
Type: Read/Write

Write Example: **EXSYNC_ENB 0x1**
Read Example: **EXSYNC_ENB ?**

1.4.67. Exsync Select (EXSYNC_SEL)

The Exsync Select (EXSYNC_SEL) command select which camera control input and active edge is used when generating exsync-triggered video patterns. The CLS-212 supports exsync triggered frame generation using any of Camera Link camera control inputs. The triggering edge is selectable as "rising" (low-to-high transition) or "falling" (high-to-low transition). See Section 1.3.8 for further information.

Parameter: EXSYNC_SEL
Settings: 0 (0x0) = CC1 rising edge
1 (0x1) = CC1 falling edge
2 (0x2) = CC2 rising edge
3 (0x3) = CC2 falling edge
4 (0x4) = CC3 rising edge
5 (0x5) = CC3 falling edge
6 (0x6) = CC4 rising edge
7 (0x7) = CC4 falling edge
Type: Read/Write

Write Example: **EXSYNC_SEL 0x7**
Read Example: **EXSYNC_SEL ?**

1.4.68. Integration Time (INTEG_TIME)

The Integration Time (INTEG_TIME) command determines the amount of time (in milliseconds) to delay the generation of video frames to simulate camera integration (exposure) characteristics. The INTEG_TIME command

may be used in both triggered (exsync) and continuous modes. See Section 1.3.5 for further information.

NOTE: ALWAYS SET REGISTER TO 0 WHEN NOT USING THIS FEATURE

Parameter: INTEG_TIME
Range: 0-65535 mS *(hex 0x0 - 0xFFF)*.
Type: Read/Write

Write Example: **INTEG_TIME 0x4000**
Read Example: **INTEG_TIME ?**

1.4.69. Linescan Mode (LINESCAN)

The Linescan Mode (LINESCAN) command places the CLS-212 in linescan mode. When linescan mode is disabled, the CLS-212 defaults to framescan mode. See Section 1.3.2 for further information.

Parameter: LINESCAN
Settings: 0 (0x0) = Framescan Mode
1 (0x1) = Linescan Mode
Type: Read/Write

Write Example: **LINESCAN 0x0**
Read Example: **LINESCAN ?**

1.4.70. DVAL State (DVAL)

The DVAL State (DVAL) command determines the static state of the Camera Link Data Valid output signal when DVAL_MODE is set to 0. See Section x.x.x for further information.

Parameter: DVAL
Settings: 0 (0x0) = DVAL output set to 0
1 (0x1) = DVAL output set to 1
Type: Read/Write

Write Example: **DVAL 0x0**
Read Example: **DVAL ?**

1.4.71. DVAL Mode (DVAL_MODE)

The DVAL Mode (DVAL_MODE) command determines the timing characteristics of the Camera Link Data Valid output signal. Settings 1-3 enable the CLS-212 to simulate oversampled (2x,4x,8x) video data which is generally used to support low pixel clock frequency cameras in Camera Link systems. See Section 1.3.5 for further information.

Parameter: DVAL_MODE
Settings: 0 (0x0) = DVAL is a static output per the DVAL command
1 (0x1) = DVAL asserted (1) every 2nd pixel clock
2 (0x2) = DVAL asserted (1) every 4th pixel clock
3 (0x3) = DVAL asserted (1) every 8th pixel clock
Type: Read/Write

Write Example: **DVAL_MODE 0x2**
Read Example: **DVAL_MODE ?**

1.4.72. Clock Disable (CLK_DIS)

The Clock Disable (CLK_DIS) command provides individual disable control for the three Channel Link transmitter chips (i.e. base, medium, full) in the Camera Link inteterface. When disabled, the associated Camera Link interface signals (i.e. clock + data) are inactive. See Sections 1.3.11 and 1.3.12 for further information.

Parameter:	CLK_DIS
Bit positions:	bit 0 = Base transmitter disabled when "1"
	bit 1 = Medium transmitter disabled when "1"
	bit 2 = Full transmitter disabled when "1"
	bit 3-7 = 0
Type:	Read/Write

Write Example: **CLK_DIS 0x7**
Read Example: **CLK_DIS ?**

1.4.73. PoCL Power Presence (POCL)

The PoCL Power Presence (POCL) command detects power presence at the Camera Link interface from a PoCL frame grabber. This register is read only. See Section 1.3.12 for further information.

Parameter:	POCL
Settings:	0 (0x0) = No PoCL power present
	1 (0x1) = PoCL power present
Type:	Read

Read Example: **POCL ?**

1.4.74. CC State (CC)

The CC State (CC) command is used to read the current state of the Camera Link camera control inputs (CC1,CC2,CC3,CC4). This register is read only. See Section 1.3.8 for further information.

Parameter: CC
Bit positions: bit 0 = CC1 (lsb)
bit 1 = CC2
bit 2 = CC3
bit 3 = CC4
bit 4-7 = 0
Type: Read

Read Example: **CC ?**

1.4.75. FPGA Version (VERSION)

The FPGA Version (VERSION) command is used to read the hardware version code for the CLS-212 Field Programmable Gate Array (FPGA) device. The standard version code is 61 (0x3D). Note that the firmware version is displayed in the startup messages.

Parameter: VERSION
Settings: 8-bit FPGA version code (48 (0x30) standard)
Type: Read

Read Example: **VERSION ?**

1.4.76. One Shot Trigger (ONE_SHOT)

The One Shot Trigger (ONE_SHOT) command enables the triggering of a single frame (or line for linescan mode) via the CLI. Note that continuous mode must be disabled to use this feature (see CONTINUOUS command). There is no read or write data associated with this command. See Section 1.3.2 for further information.

Parameter: ONE_SHOT
Settings: None, command only
Type: Command

Example: **ONE_SHOT**

1.4.77. Parameter Save (SAVE)

The Parameter Save (SAVE) command stores the current CLS-212 parameter set to non-volatile memory. The saved parameters are recalled automatically following power-up, or in response to the RECALL command. Saved parameters are maintained until altered via a subsequent SAVE command. There is no read or write data associated with this command. See Section 1.3.6 for further information.

Parameter: SAVE
Settings: None, command only
Type: Command

Example: **SAVE**

1.4.78. Parameter Recall (RECALL)

The Parameter Recall (RECALL) command retrieves the parameter set currently stored in non-volatile memory. The saved parameters are also automatically recalled during power-up initialization. There is no read or write data associated with this command. See Section 1.3.6 for further information.

Parameter: RECALL
Settings: None, command only
Type: Command

Example: **RECALL**

1.4.79. Echo Control (ECHO)

The Echo Control (ECHO) command controls CLS-212 echo-back of characters received via the control interface. Upon CLS-212 power-up, echo is enabled and the CLS-212 will echoes-back all characters received. Turning off echo disables the echo until re-enabled or a subsequent power-up reset. "ECHO ON" and "ECHO OFF" are useful in configuration files to avoid large amounts of returned data during file download. See Section 1.4 for further information.

Parameter: ECHO
Settings: ON = Enable echo (default)
OFF = Disable echo
Type: Write

Write Example: **ECHO ON**

1.4.80. Parameter Dump (DUMP)

The Parameter Dump (DUMP) command causes the CLS-212 to return the entire current parameter set to the host computer. Information is displayed in both hexadecimal and decimal format, except for SYNTH_CODE. A typical DUMP command response is shown below.

Parameter: DUMP
S-ettings: None, command only
Type: Command

Example: **DUMP**

CLS-212 Dump Example:

```
LVAL_LO    = 0x0020      / 32
LVAL_HI    = 0x0100      / 256
FVAL_LO    = 0x0002      / 2
FVAL_HI    = 0x0100      / 256
FVAL_SETUP = 0x0000      / 0
FVAL_HOLD  = 0x0000      / 0
X_OFFSET   = 0x0000      / 0
X_ACTIVE   = 0x0100      / 256
Y_OFFSET   = 0x0000      / 0
Y_ACTIVE   = 0x0100      / 256
A_PATSEL   = 0x03        / 3
B_PATSEL   = 0x00        / 0
C_PATSEL   = 0x00        / 0
D_PATSEL   = 0x00        / 0
E_PATSEL   = 0x00        / 0
F_PATSEL   = 0x00        / 0
G_PATSEL   = 0x00        / 0
H_PATSEL   = 0x00        / 0
I_PATSEL   = 0x00        / 0
J_PATSEL   = 0x00        / 0
A_FIXED    = 0x0000      / 0
B_FIXED    = 0x0000      / 0
C_FIXED    = 0x0000      / 0
D_FIXED    = 0x0000      / 0
E_FIXED    = 0x0000      / 0
F_FIXED    = 0x0000      / 0
G_FIXED    = 0x0000      / 0
H_FIXED    = 0x0000      / 0
I_FIXED    = 0x00        / 0
J_FIXED    = 0x00        / 0
```

```
A_BACK      = 0x0000      / 0
B_BACK      = 0x0000      / 0
C_BACK      = 0x0000      / 0
D_BACK      = 0x0000      / 0
E_BACK      = 0x0000      / 0
F_BACK      = 0x0000      / 0
G_BACK      = 0x0000      / 0
H_BACK      = 0x0000      / 0
I_BACK      = 0x00        / 0
J_BACK      = 0x00        / 0
A_STEP      = 0x01        / 1
B_STEP      = 0x01        / 1
C_STEP      = 0x01        / 1
D_STEP      = 0x01        / 1
E_STEP      = 0x01        / 1
F_STEP      = 0x01        / 1
G_STEP      = 0x01        / 1
H_STEP      = 0x01        / 1
I_STEP      = 0x01        / 1
J_STEP      = 0x01        / 1
A_INIT      = 0x0000      / 0
B_INIT      = 0x0000      / 0
C_INIT      = 0x0000      / 0
D_INIT      = 0x0000      / 0
E_INIT      = 0x0000      / 0
F_INIT      = 0x0000      / 0
G_INIT      = 0x0000      / 0
H_INIT      = 0x0000      / 0
I_INIT      = 0x00        / 0
J_INIT      = 0x00        / 0
CL_MODE     = 0x00        / 0
ROLL        = 0x00        / 0
SYNTH_CODE  = 0x######
FREQUENCY   = 0x14        / 20
CONTINUOUS  = 0x01        / 1
EXSYNC_ENB  = 0x00        / 0
EXSYNC_SEL  = 0x00        / 0
INTEG_TIME  = 0x0000      / 0
LINESCAN    = 0x00        / 0
DVAL        = 0x01        / 1
DVAL_MODE   = 0x00        / 0
CLK_DIS     = 0x00        / 0
POCL        = 0x0         / 0
CC          = 0x0F        / 15
VERSION     = 0x3D        / 61
```

1.5. Typical Application

A typical CLS-212 Camera Link Simulator application is shown in Figure 1-12. The CLS-212 is being used to simulate a 4-tap, 8-bit, medium configuration, area-scan camera. To support this medium configuration application, two Camera Link cables are connected between the CLS-212 and the frame grabber. Note that base configuration applications require only one cable. To control the CLS-212, the included serial cable connects the CLS-212 to a standard PC serial port. An example configuration file (cls212_example.txt) with user-selected parameters is shown in Table 1-4.

HyperTerminal (included with Windows) or other communications software program is used to download the configuration file to the CLS-212. PC serial port settings are conventional and are specified in Section 1.3.7 (9600 baud, 8 data bits, no parity, 1 stop bit, no flow control). Using HyperTerminal, the configuration file is sent to the CLS-212 by selecting the "Transfer" tab and clicking on "Send Text File". The user then specifies the location of "cls212_example.txt" and file download commences. Alternately, the parameters may be individually entered via the CLI. Subsequent changes to CLS-212 parameters can be made by downloading a new configuration file, or by manually entering commands with the keyboard.

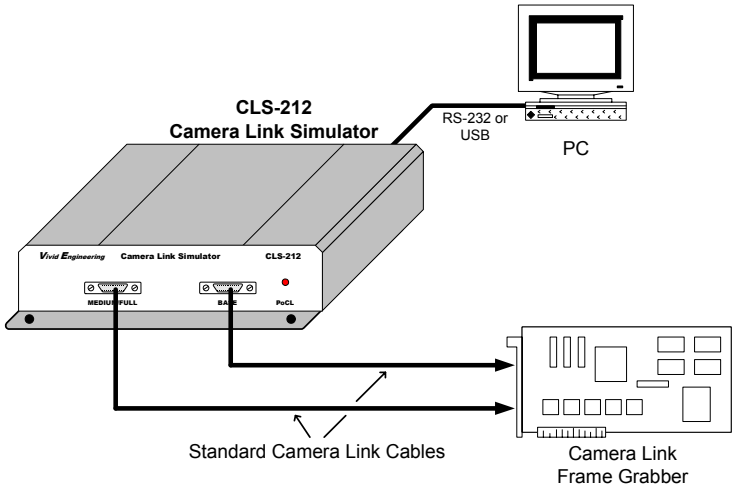


Figure 1-12: CLS-212 Typical Application

Table 1-4: Example Configuration File (cls212_example.txt)

```
//
// CLS-212 Camera Link Simulator Configuration File
//
//   Example Test Pattern Characteristics
//   - 512x512 active image area
//   - 20 MHz pixel clock rate
//   - Continuous output mode
//   - Camera Link "full" configuration
//   - Eight 8-bit pixels (8x8)
//   - Diagonal wedge pattern on all pixels


// Line Valid Low
//   - 32 clocks
LVAL_LO     32

// Line Valid High
//   - 576 clocks
LVAL_HI     576

// Frame Valid Low
//   - 2 lines
FVAL_LO     2

// Frame Valid High
//   - 512 lines
FVAL_HI     512

// Frame Valid Setup
//   - 0 clocks
FVAL_SETUP  0

// Frame Valid Hold
//   - 0 clocks
FVAL_HOLD  0

// X Offset
//   - 8 clocks
X_OFFSET    8

// X Active
//   - 512 clocks
X_ACTIVE    512

// Y Offset
//   - 0 lines
Y_OFFSET    0
```

```
// Y Active
//   - 512 lines
Y_ACTIVE    512

// Pixel A-B-C-D-E-F-G-H Pattern Select
//   - a-h = diagonal wedge = 3
A_PATSEL    3
B_PATSEL    3
C_PATSEL    3
D_PATSEL    3
E_PATSEL    3
F_PATSEL    3
G_PATSEL    3
H_PATSEL    3

// Pixel A-B-C-D-E-F-G-H Fixed Value
//   - a-h = 0
A_FIXED     0
B_FIXED     0
C_FIXED     0
D_FIXED     0
E_FIXED     0
F_FIXED     0
G_FIXED     0
H_FIXED     0

// Pixel A-B-C-D-E-F-G-H Background Value
//   - a-h = 0
A_BACK      0
B_BACK      0
C_BACK      0
D_BACK      0
E_BACK      0
F_BACK      0
G_BACK      0
H_BACK      0

// Pixel A-B-C-D-E-F-G-H pattern step size
//   - a-h = 1 = patterns increment by 1
A_STEP      1
B_STEP      1
C_STEP      1
D_STEP      1
E_STEP      1
F_STEP      1
G_STEP      1
H_STEP      1

// Camera Link Mode
//   - mode = full 8x8 = 15
CL_MODE     15
```

```
// Pattern Roll
//   - roll disabled = 0
ROLL        0

// Clock Synthesizer Code
//   - Not used, using Clock Frequency instead
// SYNTH_CODE  0x33543D

// Clock Frequency
//   - 20 MHz
FREQUENCY   20

// Continuous Mode
//   - continuous mode enabled = 1
CONTINUOUS  1

// Exsync Enable
//   - exsync triggering disabled = 0
EXSYNC_ENB  0

// Exsync Select
//   - CC1 rising edge = 0
EXSYNC_SEL  0

// integration time
//   - 0 = 0 mS delay = disabled
INTEG_TIME  0

// Linescan Mode
//   - linescan mode disabled = framescan mode = 0
LINESCAN    0

// DVAL State
//   - dval signal state = 1
DVAL        1//   - 20//   - 512x512 active image area
```

1.6. Specifications

Table 1-5: CLS-212 Specifications

Feature	Specification
Camera Interface	Camera Link "base/medium/full" w/ 80-bit + PoCL
Camera Connectors	26-pin SDR (miniCL) type (2)
Frequency Range	20-85 MHz
Serial Port Interface	RS-232
Serial Port Connector	Male 9-pin D-Sub (DB9)
Serial Port Cable	3 meter DB9 female - DB9 female null modem cable
USB Port	Via external USB to serial RS-232 adapter (optional)
Chipset	National Semi. DS90CR287 (2)
Power Supply	Universal wall style w/ US & Europe outlet plugs
Power Jack	2.1 x 5.5 mm, center-positive
Power Requirements	5-7 VDC, 700 mA (typical)
Cabinet Dimensions	5.28" (L) x 1.18" (H) 7.12" (D)
Weight	16 oz
Operating Temperature Range	0 to 50° C
Storage Temperature Range	-25 to 75° C
Relative Humidity	0 to 90%, non-condensing

2. Interface

2.1. Front Panel Connections

The CLS-212 Camera Link Simulator front panel is shown in Figure 2-1. The front panel contains two video connectors for connecting to the frame grabber. Camera Link "medium" & "full" configurations utilize both video connectors. "Base" configurations utilize only the "base" connector.

The camera connectors are "miniCL" 26-pin SDR type (SDR-26), 3M p/n 12226-8250-00FR w/ 3M p/n 12600-S-112 jack screws. Figure 2-2 identifies the SDR-26 pin positions.

The front panel also includes a PoCL power presence indicator.

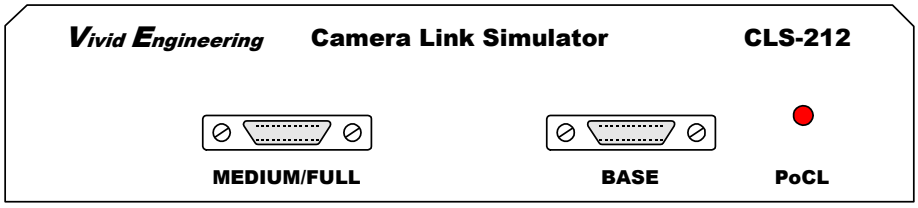


Figure 2-1: CLS-212 Front Panel

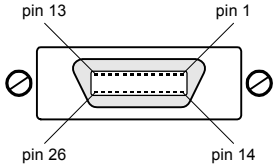


Figure 2-2: SDR-26 (miniCL) Connector Pin Positions

2.1.1. Camera Connector Signals

The SDR-26 camera connector signal assignments are compliant with the Camera Link Specification for the "base", "medium", and "full" configurations. The "base" connector is also PoCL compliant.

Table 2-1 and 2-2 identify the signal assignments for the SDR-26 (miniCL) "base" and "medium/full" camera connectors, respectively.

Note that the connector pin assignments are as defined for the camera interface in the Camera Link Specification. This provides compatibility with standard Camera Link cables

2.1.2. Cable Shield Grounding

Camera Link cable "outer" shields are connected to the CLS-212 aluminum case. The case is isolated from the CLS-212 circuitry and the cable "inner" shields.

The frame grabber cable "inner" shield connects to circuit digital ground, maintaining signal reference levels between the CLS-212 and the frame grabber.

Table 2-1: CLS-212 "Base" Connector

Camera Link Signal Name	"Base" Connector Pin # (camera pinout)	Signal Direction	Notes
Standard=inner shield PoCL=+12v power	1	N/A	*tied to 10K sense resistor (+)*
Standard=inner shield PoCL=power gnd	14	N/A	*tied to 10K sense resistor (-)*
X0-	2	CLS-212 → FG	
X0+	15	CLS-212 → FG	
X1-	3	CLS-212 → FG	
X1+	16	CLS-212 → FG	
X2-	4	CLS-212 → FG	
X2+	17	CLS-212 → FG	
Xclk-	5	CLS-212 → FG	
Xclk+	18	CLS-212 → FG	
X3-	6	CLS-212 → FG	
X3+	19	CLS-212 → FG	
SerTC+	7	FG → CLS-212	*serial comm*
SerTC-	20	FG → CLS-212	*"*
SerTFG-	8	CLS-212 → FG	*serial comm*
SerTFG+	21	CLS-212 → FG	*"*
CC1-	9	FG → CLS-212	
CC1+	22	FG → CLS-212	
CC2+	10	FG → CLS-212	
CC2-	23	FG → CLS-212	
CC3-	11	FG → CLS-212	
CC3+	24	FG → CLS-212	
CC4+	12	FG → CLS-212	
CC4-	25	FG → CLS-212	

Standard=inner shield PoCL=power gnd	13	N/A	*tied to 10K sense resistor (-)*
Standard=inner shield PoCL=+12v power	26	N/A	*tied to 10K sense resistor (+)*

"FG" = Frame Grabber

Table 2-2: CLS-212 "Medium/Full" Connector

Camera Link Signal Name	"Medium/Full" Connector Pin # (camera pinout)	Signal Direction	Notes
Inner shield	1	N/A	*tied to digital ground*
Inner shield	14	N/A	*tied to digital ground*
Y0-	2	CLS-212 → FG	
Y0+	15	CLS-212 → FG	
Y1-	3	CLS-212 → FG	
Y1+	16	CLS-212 → FG	
Y2-	4	CLS-212 → FG	
Y2+	17	CLS-212 → FG	
Yclk-	5	CLS-212 → FG	
Yclk+	18	CLS-212 → FG	
Y3-	6	CLS-212 → FG	
Y3+	19	CLS-212 → FG	
100 ohm	7	N/A	*100 ohm termination, 7-20*
terminated	20	N/A	*100 ohm termination, 7-20*
Z0-	8	CLS-212 → FG	
Z0+	21	CLS-212 → FG	
Z1-	9	CLS-212 → FG	
Z1+	22	CLS-212 → FG	
Z2-	10	CLS-212 → FG	
Z2+	23	CLS-212 → FG	
Zclk-	11	CLS-212 → FG	
Zclk+	24	CLS-212 → FG	
Z3-	12	CLS-212 → FG	
Z3+	25	CLS-212 → FG	
Inner shield	13	N/A	*tied to digital ground*

Inner shield	26	N/A	*tied to digital ground*

"FG" = Frame Grabber

2.2. Rear Panel

The CLS-212 Camera Link Simulator rear panel is shown in Figure 2-3. The rear panel contains an RS-232 connector, power on indicator, on-off switch, and DC power jack. The DC power jack accepts 5-7 volts DC, center-positive.

The RS-232 serial port connector is a standard 9-pin male D-Sub type (DB9), Tyco p/n 5747840-4. Figure 2-4 identifies the DB9 pin positions.

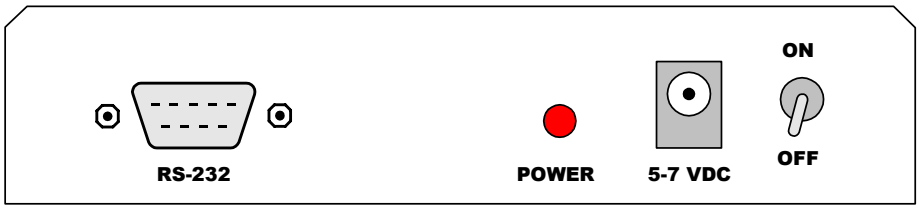


Figure 2-3: CLS-212 Rear Panel

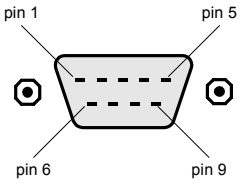


Figure 2-4: DB9 Connector Pin Positions

2.2.1. DB9 Connector Signals

The DB9 connector signal assignments are compliant with the RS-232 serial interface standard. Table 2-3 identifies the DB9 signal assignments.

Table 2-3: DB9 Connector

RS-232 Signal Name	DB9 Pin#	Signal Direction	Notes
Received Line Signal Detect	1	N/A	*tied to pins 4 & 6*
Received Data	2	PC → CLS-212	
Transmitted Data	3	CLS-212 → PC	
Data Terminal Ready	4	N/A	*tied to pins 1 & 6*
Signal Ground (common)	5	N/A	*tied to digital ground*
DCE Ready	6	N/A	*tied to pins 1 & 4*
Request To Send	7	N/A	*tied to pin 8*
Clear To Send	8	N/A	*tied to pin 7*
Ring Indicator	9	N/A	*no connection*

"PC" = Control PC, workstation, or terminal

3. Mechanical

3.1. Dimensions

The CLS-212 Camera Link Simulator cabinet dimensions are shown in Figure 3-1.

The CLS-212 is housed in a sturdy aluminum enclosure. The body is extruded aluminum, with detachable front and rear endplates. The enclosure incorporates a mounting flange. The flange contains four predrilled holes (0.15" diameter) for convenient equipment mounting. A mounting drawing is provided in Figure 3-2.

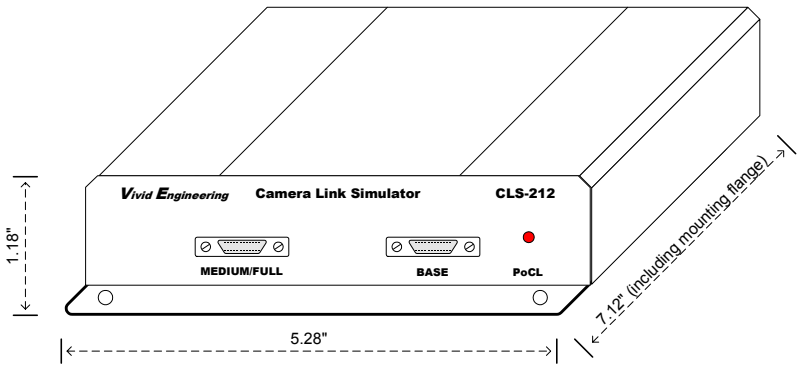


Figure 3-1: CLS-212 Cabinet Dimensions

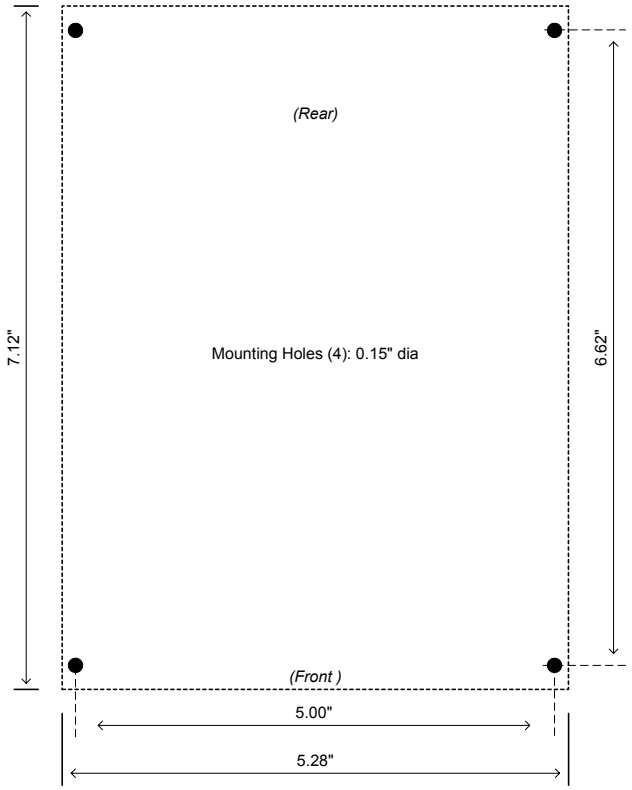


Figure 3-2: Mounting Holes

3.2. External Power Supply

The CLS-212 is powered by 5-7 VDC and incorporates a standard 2.1 x 5.5 mm DC power jack. Power plug polarity is center-positive.

The CLS-212 includes a multi-nation wall-mount power supply that handles a wide power range (90-264 VAC, 47-63 Hz) and comes with a set of outlet plugs suitable for most countries (US, Europe, UK, etc). The CLS-212 may also be purchased without the power supply.

The CLS-212 is protected by an internal resetable fuse.

4. Appendix

4.1. Full Configuration Examples

The following four examples show the key configuration settings used to generate Camera Link "full" configuration test patterns. In Camera Link full configuration, eight 8-bit pixels are simultaneously output with every pixel clock. This supports very high frame rates. Camera Link full configuration cameras generally output eight consecutive (sequential) pixels in the line. For this reason, camera horizontal dimension is a multiple of 8.

A 256x256 image is used for our examples. Since 8 consecutive pixels are output with every pixel clock, the horizontal line is only 32 clocks in duration, plus horizontal blanking. The "A" configuration registers are used to specify the 1st pixel, the "B" configuration registers for the 2nd pixel, continuing to the "H" configuration registers for the 8th pixel.

4.1.1. 8-Bit 8-Tap Horizontal Wedge Example

Objective: Horizontal wedge, 8-bit monochrome, 256x256 image size,

8-bit x 8-tap (Camera Link Full)

Key Parameters:

LVAL_HI	32
FVAL_HI	256
X_ACTIVE	32
Y_ACTIVE	256
A-H PATSEL	1
A-H STEP	8
A_INIT	0
B_INIT	1
C_INIT	2
D_INIT	3
E_INIT	4
F_INIT	5
G_INIT	6
H_INIT	7
CL_MODE	15

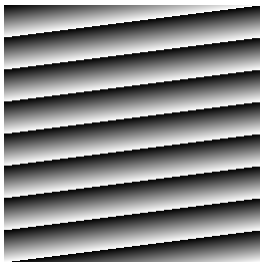
Comments: Eight consecutive pixels are output every pixel clock, so line valid (LVAL_HI) time is 256/8 = 32. Initial value (INIT) and step size (STEP) settings produce a normal gradient (0,1,2…255).

4.1.2. 8-Bit 8-Tap Vertical Wedge Example

Objective:	Vertical wedge, 8-bit monochrome, 256x256 image size,	
	8-bit x 8-tap (Camera Link Full)	
Key Parameters:	LVAL_HI	32
	FVAL_HI	256
	X_ACTIVE	32
	Y_ACTIVE	256
	A-H PATSEL	2
	A-H STEP	1
	A-H INIT	0
	CL_MODE	15
Comments:	Eight consecutive pixels are output every pixel clock, so line valid (LVAL_HI) time is 256/8 = 32. Normal gradient (0,1,2…255) is generated.	

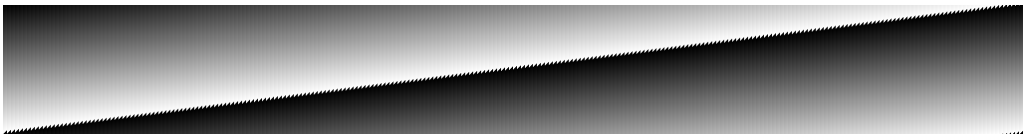
4.1.3. 8-Bit 8-Tap Diagonal Wedge Example #1

Objective: size,	Diagonal wedge, 8-bit monochrome, 256x256 image	
	8-bit x 8-tap (Camera Link Full)	
Key Parameters:	LVAL_HI	32
	FVAL_HI	256
	X_ACTIVE	32
	Y_ACTIVE	256
	A-H PATSEL	3
	A-H STEP	8
	A_INIT	0
	B_INIT	1
	C_INIT	2
	D_INIT	3
	E_INIT	4
	F_INIT	5
	G_INIT	6
	H_INIT	7
	CL_MODE	15
Comments:	Eight consecutive pixels are output every pixel clock, so line valid (LVAL_HI) time is 256/8 = 32. Initial value (INIT) and step size (STEP) settings produce a normal gradient in the X direction (0,1,2…255), but the Y direction gradient is 0,8,16… due to the STEP setting.	



4.1.4. 8-Bit 8-Tap Diagonal Wedge Example #2

Objective: size,	Diagonal wedge, 8-bit monochrome, 2048x256 image	
	8-bit x 8-tap (Camera Link Full)	
Key Parameters:	LVAL_HI	256
	FVAL_HI	256
	X_ACTIVE	256
	Y_ACTIVE	256
	A-H PATSEL	3
	A-H STEP	1
	A_INIT	0
	B_INIT	1
	C_INIT	2
	D_INIT	3
	E_INIT	4
	F_INIT	5
	G_INIT	6
	H_INIT	7
	CL_MODE	15
Comments:	Eight consecutive pixels are output every pixel clock, so line valid (LVAL_HI) time is 2048/8 = 256. Initial value (INIT) and step size (STEP) settings produce an X-direction gradient of the form 0,1,2,3,4,5,6,7, 1,2,3,4,5,6,7,8, 2,3,4,5,6,7,8,9, … Y-direction gradient is normal (0,1,2…255).	



4.2. 80-bit Examples

The following four examples show the key configuration settings used to generate Camera Link test patterns for the newer 80-bit configurations. Two 80-bit configurations exist; ten 8-bit taps, and eight 10-bit taps. The examples provided are for ten 8-bit taps, also known as Deca Configuration.

In the Deca configuration, ten 8-bit pixels are simultaneously output with every pixel clock. This supports very high frame rates. Deca configuration cameras generally output ten consecutive (sequential) pixels in the line. For this reason, camera horizontal dimension is a multiple of 10.

A 320x256 image is used for our examples. Since 10 consecutive pixels are output with every pixel clock, the horizontal line is only 32 clocks in duration, plus horizontal blanking. The "A" configuration registers are used to specify the 1st pixel, the "B" configuration registers for the 2nd pixel, continuing to the "J" configuration registers for the 10th pixel.

4.2.1. 8-Bit 10-Tap Horizontal Wedge Example

Objective: Horizontal wedge, 8-bit monochrome, 320x256 image size,

8-bit x 10-tap (Camera Link Full, 80-bit DECA)

Key Parameters:

LVAL_HI	32
FVAL_HI	256
X_ACTIVE	32
Y_ACTIVE	256
A-J PATSEL	1
A-J STEP	8
A_INIT	0
B_INIT	1
C_INIT	2
D_INIT	3
E_INIT	4
F_INIT	5
G_INIT	6
H_INIT	7
I_INIT	8
J_INIT	9
CL_MODE	13

Comments: Ten consecutive pixels are output every pixel clock, so line valid (LVAL_HI) time is 320/10 = 32. Initial value (INIT) and step size (STEP) settings produce a gradient of the form 0,1,2,3,4,5,6,7,8,9, 8,9,10,11,12,13,14,15,16,17, 16,17,18,19,20,21,22,23,24,25, …

4.2.2. 8-Bit 10-Tap Vertical Wedge Example

Objective: size,	Vertical wedge, 8-bit monochrome, 320x256 image	
	8-bit x 10-tap (Camera Link Full, 80-bit DECA)	
Key Parameters:	LVAL_HI	32
	FVAL_HI	256
	X_ACTIVE	32
	Y_ACTIVE	256
	A-J PATSEL	2
	A-J STEP	1
	A-J INIT	0
	CL_MODE	13
Comments:	Ten consecutive pixels are output every pixel clock, so line valid (LVAL_HI) time is 320/10 = 32. Normal gradient (0,1,2…255) is generated.	

4.2.3. 8-Bit 10-Tap Diagonal Wedge Example #1

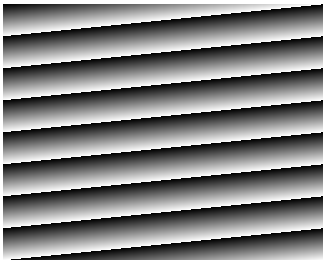
Objective: Diagonal wedge, 8-bit monochrome, 320x256 image size,

8-bit x 10-tap (Camera Link Full, 80-bit DECA)

Key Parameters:

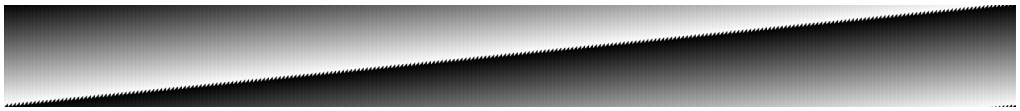
LVAL_HI	32
FVAL_HI	256
X_ACTIVE	32
Y_ACTIVE	256
A-J PATSEL	3
A-J STEP	8
A_INIT	0
B_INIT	1
C_INIT	2
D_INIT	3
E_INIT	4
F_INIT	5
G_INIT	6
H_INIT	7
I_INIT	8
J_INIT	9
CL_MODE	13

Comments: Ten consecutive pixels are output every pixel clock, so line valid (LVAL_HI) time is 320/10 = 32. Initial value (INIT) and step size (STEP) settings produce an X-direction gradient of the form 0,1,2,3,4,5,6,7,8,9, 8,9,10,11,12,13,14,15,16,17, 16,17,18,19,20,21,22,23,24,25, …
Y direction gradient is 0,8,16… due to the STEP setting.



4.2.4. 8-Bit 10-Tap Diagonal Wedge Example #2

Objective:	Diagonal wedge, 8-bit monochrome, 2560x256 image size,	
	8-bit x 10-tap (Camera Link Full, 80-bit DECA)	
Key Parameters:	LVAL_HI	32
	FVAL_HI	256
	X_ACTIVE	32
	Y_ACTIVE	256
	A-J PATSEL	3
	A-J STEP	1
	A_INIT	0
	B_INIT	1
	C_INIT	2
	D_INIT	3
	E_INIT	4
	F_INIT	5
	G_INIT	6
	H_INIT	7
	I_INIT	8
	J_INIT	9
	CL_MODE	13
Comments:	Ten consecutive pixels are output every pixel clock, so line valid (LVAL_HI) time is 320/10 = 32. Initial value (INIT) and step size (STEP) settings produce an X-direction gradient of the form 0,1,2,3,4,5,6,7,8,9, 1,2,3,4,5,6,7,8,9,10, 2,3,4,5,6,7,8,9,10,11,… Y-direction gradient is normal (0,1,2…255).	



5. Revision History

Table 5-1: CLS-212 User's Manual Revision History

Document ID #	Date	Changes
200483-1.0	6/30/2010	Initial release of manual